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Co-author(s):	Frederico Augusto Pinho Haasis (CEPEL), Cesar Jorge Bandim (CEPEL)
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23/01/2023	v1.2	Oscar Solano Rueda (CEPEL)	Final version

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List of Abbreviations

AFE	Active Front End (Triphase converter)
ALTM	Advanced Laboratory Testing Method
CO	Project Coordinator
CEPEL	Centro de Pesquisas de Energia Elétrica (electrical energy research center -Brazil)
DG	Distributed Generators
DER	Distributed Energy Resources
EC	European Commission
ESP Lab	Electrical Sustainable Power Lab
HMI	Human Machine Interface
HUT	Hardware under test
LA	Lab Access
PA	Power Amplifier
PHIL	Power Hardware-in-the-loop
PLL	Phase locked loop
pu	per unit
PV	Photovoltaic
RTS	Real-time Digital Simulator
SIRFN	Smart Grid International Research Facility Network
UG	User Group
UP	User Project

Executive Summary

Power Hardware-in-the-loop (PHIL) testing has emerged as an appropriate validation approach for electrical systems. PHIL set-ups provide an environment for repeatable, economical, flexible, and scalable hardware and software verification under realistic conditions. However, PHIL set-ups are complex systems which design, and hardware components significantly influence its results. Therefore, a potential concern is the replicability of PHIL results over different lab infrastructures. In that context, this work aims to investigate the aspects related to the PHIL results replicability through analysis of the behavior of a same case of study in two different PHIL set-ups.

Lab Access (LA) User Group (UG) works at CEPEL's Smart Grid laboratory (Lab SG), a recent inaugurated infrastructure located in Brazil, that has, within its resources, a PHIL test bench composed by one digital real-time simulator (OPAL-RT), two linear amplifiers (Spitzenberger & Spies) and three programable inverters (Triphase). Part of these devices were used, before LA period, to stablish a PHIL set-up for distributed PV generation integration analysis in which an IEEE benchmark feeder interacts with a real inverter that represents PV generation (HUT – Hardware under test). The tests performed at CEPEL Lab focused on voltage profile behavior, using the Brazilian standard for power quality in distribution grids as the main standard reference.

During the 4 weeks of LA period detailed in this report, a replicated PHIL set-up was established using Host Laboratory (ESP Lab) infrastructure, in which experimental simulations of two test cases were carried out. A set of real electrical measurements and virtual variables were obtained as results of the performed test. This report presents a broad description of the main hardware and software configurations as well as the differences between both set-ups. LA period was also used to implement a simplifier PF closed loop control in which active and reactive power references are sent to HUT, to implement an ancillary service for voltage profile control. This control was replicated at CEPEL Lab after LA period.

Preliminary findings

- Even though ESP Lab's PHIL set-up significatively differs from the one available at CEPEL Lab, both set of results lead to the same conclusion regarding PV hosting capability levels due to overvoltage issues.
- The implemented PF control loop proved to be appropriate, for the given modeled grid, to avoid overvoltage deviations.
- It was not possible verify the reproducibility of CEPEL's and ESP lab's results at waveform-comparison level because of the relevant differences between both PHIL set-ups. As: i) four-wire equipment (CEPEL) vs three-wire equipment (ESP Lab), ii) interface algorithm based on instantaneous variables (CEPEL) vs interface algorithm with rms quantities (ESP Lab) and iii) non-real time MODBUS communication for PF control set-point establishment (CEPEL) vs Aurora real time communication (ESP Lab).

Open threads:

- Change of the electrical model represented at the RTS for one that can be fully represented by ESP Lab, for instance, with no unbalanced voltages and currents.
- Modification of internal Triphase converter controllers to have the same set of adjustments in both PHIL set-ups.

1 Lab-Access User Project Information

1.1 Overview

USER PROJECT	
User Project Acronym	PHIL-Rep
User Project Title	Ensuring Replicability of Power HIL Simulations: A Proposal to-wards comparable PHIL Tests
ERIGrid Reference	146
ERIGrid 2.0 TA Call No.	5th Call

HOST RESEARCH INFRAESTRUCTURE			
Name	Electrical Sustainable Power Lab (ESP Lab - TU Delft)		
Country	Netherlands		
Start date	12/09/2022	No. of access days	20
End date	07/10/2022	No. of stay days	30

USER GROUP	
Name (Leader)	Oscar Antonio Solano Rueda
Organization	Centro de Pesquisas de Energia Elétrica (CEPEL)
Country	Brazil

1.2 Research Motivation, Objectives, and Scope

It is well known that electrical distribution grids around the world are experimenting an accelerated increase on the insertion of converter-based generation. In the Brazilian case, as an example, photovoltaic generation has reached, in November/2022, an installed capacity superior to 21 GWp, which is more than four times bigger the one installed at the end of 2019 (ABSOLAR, 2022). In this scenario, the provision of ancillary services functions by distributed generators (DG) is considered as an important element of future (smart) grids.

Power Hardware-in-the-loop (PHIL) test benches have emerged as an appropriate testing and validation environment for DER (Distributed Energy Resources) ancillary services. However, PHIL simulation consists in complex systems that are not fully acknowledged by the stakeholders in the electrical sector, especially in the case of developing countries like Brazil. Additionally, it is known that PHIL test bench design and components significantly influence its results (Lauss et al., 2016). Therefore, the following question arises: How to ensure PHIL results are replicable in different test benches?

The aim of the current research is to contribute answering that question by replicating a PHIL simulation scenario carried out at UG organization (CEPEL), using the host research infrastructure (Electrical Sustainable Power Lab). It is worth highlight that ESP Lab's PHIL test bench contains a set of components and arrangements different than the ones available at CEPEL's laboratory.

It is within the scope of this research: i) to implement the PHIL test bench at host research lab, which includes hardware and software configurations; ii) to perform a set of experimental tests, iii) to adjust CEPEL's test bench form the insights obtained by the access period, iv) to compare quantitatively and qualitatively the pair of results, and v) to present a set of recommendations

to achieve interlaboratory PHIL testing replicability.

1.3 Structure of the Document

This document is structured as follows: Section 2 briefly outlines the state-of-the-art of PHIL simulations and its importance as a recent technique for experimental testing and system-level validation of smart grids solutions. Section 3 presents the test plan, procedure and PHIL set-up employed during Lab Access (LA) period. Once this work discusses PHIL replicability between CEPEL and ESP Lab test benches, both set-ups are described, with more focus on ESP Lab infrastructure. In Section 4 the results of the performed experiments are presented as well as the conclusion of LA activities. Finally, in Section 5 the potential open issues and suggestion for improvements are discussed.

2 State-of-the-Art/State-of-Technology

Power Hardware-in-the-loop testing has emerged in the last decade as a tool to address the challenges caused by the insertion of new assets in the grids, as intermittent distributed generation, distributed storage, and electric vehicle connections, among others, collectively referred to as DER. PHIL can be defined as a set-up where real-time simulation is combined with physical Hardware (HUT) in a closed loop interaction in which there is real power flow through the HUT, which implies the use of a power amplifier, which absorbs or generates power (de Jong et al., 2012).

PHIL test benches have been used in a variety of applications. In (Torres et al., 2021), for instance, a PHIL set-up evaluated the performance of various control strategies for dynamic frequency support fast active power regulation (FAPR). (Nelson et al., 2016) uses PHIL testing to evaluate the impact of grid support PV inverters to be applied at Hawaiian electrical system. (Kotsampopoulos et al., 2012) presents the design and development of a PHIL environment used to analyze the voltage profile of PV generation as result of solar irradiation variations.

Three main hardware components compose a PHIL set-up: i) real-time digital simulator (RTS), ii) power amplifier (PA) and iii) HUT. These devices are costly, and its use is not simple, which narrows the number PHIL test bench users. In the Brazilian case, for example, it is not known that any institution other that CEPEL owns an operative PHIL set-up. In this context, and considering that PHIL simulation could suffer of bandwidth, accuracy, and stability issues (Lauss et al., 2016; Tremblay et al., 2017), the establishing of technical groups that work collaborative to define standards / better practices that impulse PHIL testing adoption for the electrical stakeholders is highly relevant.

One of the more important international collaboration platforms is SIRFN (Smart Grid International Research Facility Network), coordinated by DERlab, which works in four focus areas, among them “Advanced Laboratory Testing Methods - ALTM” (Brundlinger et al., 2015). In (Montoya et al., 2020), SIRFN ALTM members published an extensive survey of smart grid research facilities including the description of their control - HIL, Power - HIL and Power System in the loop test benches, and describing its main application uses. It is worth highlight that the list of experiments carried out by SIRFN members cite equipment used by each one of them, which are different given the bunch of components vendors.

In 2013, the Distributed Energy Research Infrastructures (DERri) published a report on harmonization of rules for PHIL experiments (T. Strasser et al., 2013), which defined common reference models for DER components modelling and described the procedure steps used for PHIL simulation in the different lab infrastructures, both activities have the focus of pursuing standardization between the DERri partners. The first stage of Erigrid project also contribute to the efforts of standardization of PHIL testing. (T. I. Strasser et al., 2020) summarises its main achievements and introduces a holistic approach for laboratory evaluation of complex systems. Finally, it is relevant to highlight the creation of the IEEE WG 2004, in 2017, that is focused on defining established practices for the use of PHIL simulation.

A type of validation that has been outside of the major focus of the mentioned previous works is to evaluate the replicability of the same PHIL simulation case study in two or more research infrastructures, as proposed in the current Application. This kind of verification is within the focus of the current research.

3 Executed Tests and Experiments

3.1 Test Plan, Standards, Procedures, and Methodology

As mentioned before, the current work attempts to replicate a case study previously developed at CEPEL's Smart Grids lab, however using ESP Lab's resources. In this sense, it is worth noting that **this report is richer in details regarding the modelling at ESP Lab, during LA period**, in comparison with the developments at CEPEL Lab. The case study consists of medium power PV integration into an IEEE benchmark distribution grid. The main characteristic of hardware and software set-ups are presented in Section 3.2.

Within the resources of the real time simulation infrastructure of ESP Lab at TU Delft, the following were used for the LA Project:

- RTDS® real time digital simulator: Two Novacor racks + Aurora protocol interface.
- Triphase programable inverter (AC/DC/AC, 15 kW, 0..440 V, 3 x 24 A), working as power amplifier for the PHIL set-up.
- Triphase programable inverter (DC/AC, 15 kW, 0..440 V, 3 x 24 A), working as HPUT.

These devices are located at different rooms into ESP Lab layout, which count with one for real-time computation devices and the other one for power devices (Triphase inverters and it controls), however they are interconnected in terms of digital communication, via an Aurora protocol link over an optic fiber cable. Figure 1 presents a couple of pictures of both lab rooms, taken during LA period.

(a) (b)

Figure 1: ESP Lab's resources used. a) RDTS room, b) power devices room.

3.1.1 Test Plan

It is worth highlighting that one the activities within the scope of this project consist in the establishment of the PHIL set-up at ESP Lab, which requires both hardware and software configurations, whose details are presented in Section 3.2. Thus, only after finishing its implementation and start-up the system was available for experimental testing. Table 1 presents a description of the main activities performed during LA period. Two test cases were implemented, as shown next, each case is composed by a couple of operation points.

- Test case 1 – power injection with PF = 1
- Test case 2 – power injection with automatic PF control, given by a close loop control routine executed at RTS

In the previous list, test case 1 was already defined in the project proposal. Test case 2 was defined together with ESP Lab researchers and implemented for ESP Lab PHIL test bench during the LA period. Therefore, in order to evaluate replicability, the corresponding adjustments were implemented at CEPEL's lab after finishing the LA period. This approach agrees with the holistic test procedure presented on (T. I. Strasser et al., 2020), where the introduction of automatic PF control could be interpreted as a procedure refinement.

Table 1: Project activities schedule.

Date	Activity
Before ERIGrid 2.0 LA period	Implementation of case study at CEPEL Laboratory, performing of Test case 1
Week 1	Safely training by ESP Lab technician, Definition of hardware set-up at ESP Lab, Electrical configuration, First model developments at RSCAD software.
Week 2	Basic PHIL experiment considering a simplifier electrical system.
Week 3	IEEE 34 modelling at RSCAD Performing of Test case 1
Week 4	Implementation of automatic PF control strategy. Performing of Test case 2, Preparation and execution of demonstration for ESP Lab members.
After ERIGrid 2.0 LA period	Adequations at CEPEL to allow the performing of Test case 2.

3.1.2 Standards and procedures

The case study selected in this research focuses on the analysis of steady state voltage violations over the simulated distribution network that is evaluated using Brazilian energy quality standard (ANEEL, 2018). This standard categorizes the steady state voltages levels as "adequate", "precarious", and "critical" in function of the measurement voltage, as depicted in the Table 2, below.

Table 2: Classification of steady state voltage at system with nominal voltage between 1 kV and 69 kV, according to PRODIST.

Classification	Voltage level in pu of nominal
Adequate	$0.93 \leq V_{mea} \leq 1.05$
Precarious	$0.90 \leq V_{mea} \leq 0.93$
Critical	$V_{mea} \leq 0.90 \; or \; V_{mea} > 1.05$

On the other hand, the execution of each PHIL simulation at ESP Lab follows a defined procedure. Test case 1 follows the sequence:

i. Starting of real time model simulation at RSCAD Runtime. As initial condition the Interface Algorithm's "close loop" binary input (see Section 3.2.3) is turned OFF.
ii. Starting of Power Amplifier. Triphase's PA operation is conducted via Matlab/Simulink interface, using a set of factory-defined sequence commands to correctly close the internal contacts and start the control loops, as defined in its documentation. At the end of this turn-on the PA AC output generates a set of three phases voltages which amplitude, frequency and phase are controlled by the model being simulated ad RTS.
iii. Starting of HUT operation, via Matlab/Simulink. Like the previous step, there is a factory-defined sequence of commands that ends with the HUT injecting the current references into PA. In this work, AC current references are stablished manually at

Matlab/Simulink and represents the PV generation power injection. As initial condition, the HUT current injection is stablished as zero.

iv. Turning ON of the Interface Algorithm's "close loop" binary input, closing the loop between real and simulated environments.

v. Increasing of HUT current injection (i_{HUT}) from zero to 5 A, which causes that RTS model interprets the feedback current as a power injection of about 160 kW at the Point of Common Coupling (PCC), with unity power factor.

vi. Setting up of RSCAD's "plot update" trigger, used to acquire voltage and currents waveforms during the transients.

vii. Increasing of HUT current injection to 22 A (≈740 kW), which causes a voltage violation considering the limits of Table 2, and a triggered waveform acquisition.

Test Case 2 follows all the steps described above together with the next ones:

viii. Enabling of the automatic FP control (described in Section 3.2.2). This control causes PV generation changes from unity power factor to the one required to bring back voltage profiles to Adequate levels according to Table 2.

ix. Decreasing of HUT current injection back to 5 A, which causes voltage reductions and leads to FP modifications at PV inverter, turning back to unity power factor.

3.1.3 Methodology

Figure 2 presents the PHIL testing flowchart used. As depicted, it is a closed loop where HUT currents are measured and sent back as input for RTS simulation where the voltage at PCC are determined. The detailed set up is described in Section 3.2, similarly Figure 5 presents a flowchart with the PF control strategy employed. The test bench interacts with two sets of user's inputs: i) a binary variable that enables/disables the PF control and ii) HMI HUT currents reference for direct and quadrature axis I_d^{HMI} and I_q^{HMI}.

Two kinds of results are obtained from the tests performed in this research: i) real electrical measurements and ii) simulated variables. The first ones are obtained from the PA-HUT set, which have voltage and currents sensors which measurements are sent to RTS. The second ones are obtained internally at RTS as results of the iteration of the simulated model with HUT behavior. Therefore, all the measurements are available at RTS, and it is possible to export them to different file formats. In this work it .csv files are used. After test plan execution at ESP Lab, the results are compared with the ones obtained at CEPEL lab.

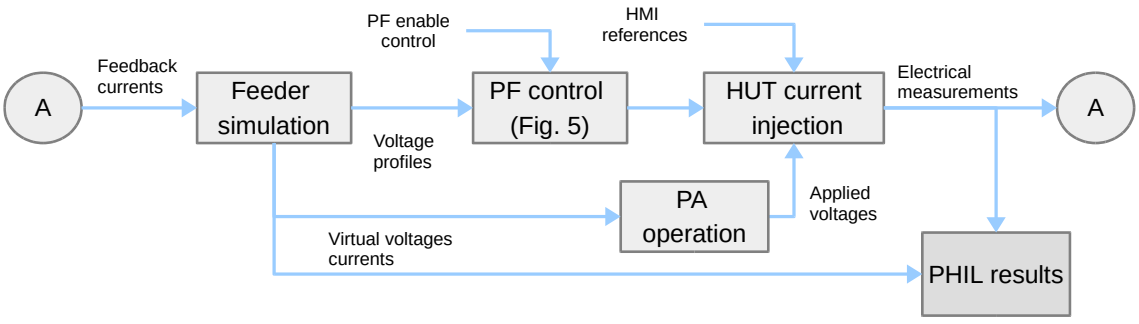

Figure 2: Tests flowchart.

The focus of this study case is to identify voltage violations over the entire distribution feeder. This work aims to demonstrate that PV generation could cause quality energy deviations different than PCC. Additionally, the experimental validation seeks to demonstrate the operation of a simple ancillary service to avoid unwanted consequences from distributed generation.

Regarding PHIL replicability verification, Section 3.2.4 brings an overview of the implementation differences between both PHIL set-ups. A qualitatively comparison is realized focused on the main operative conclusions that could be obtained for each PHIL set-up.

3.2 Test Set-up(s)

3.2.1 Hardware set-up

Figure 3 shows a schematic diagram of PHIL Hardware set-up at ESP Lab. It is possible to identify the role of each one of the resources used in this project, listed in Section 3.1.

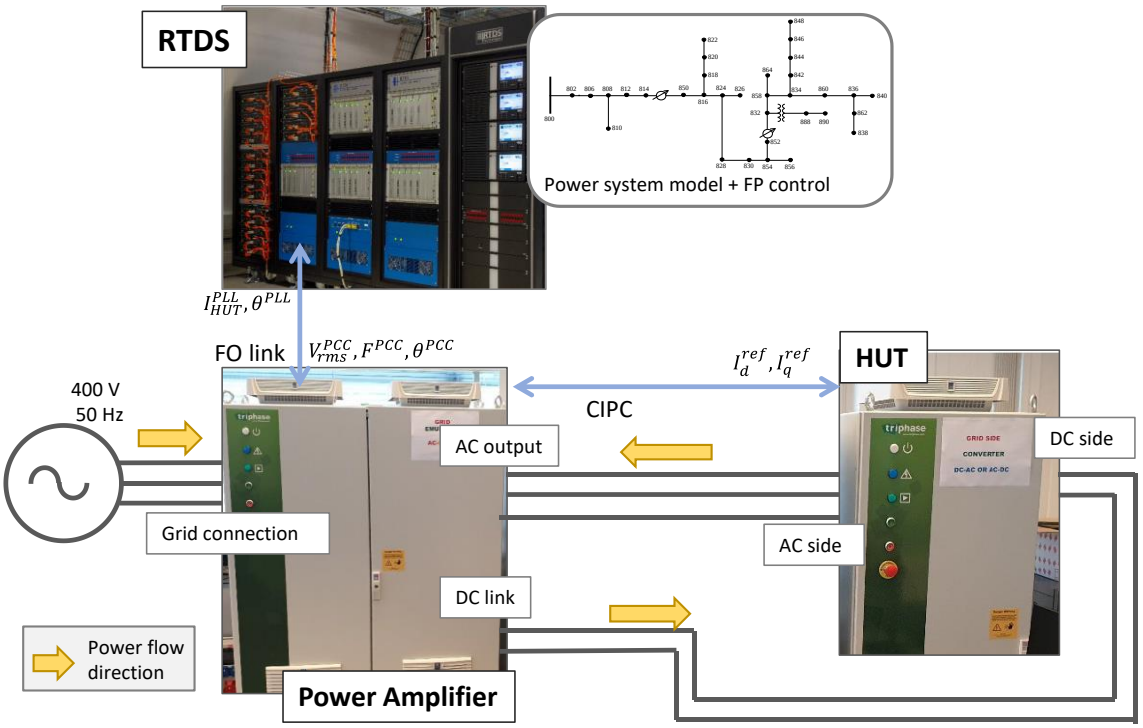

Figure 3: PHIL Hardware set-up at ESP Lab.

RTDS® executes the real time simulation of IEEE 34 bus distribution system benchmark (IEEE PES AMPS DSAS Test Feeder Working Group, 2017), which is a well-known 24,9 kV system adapted from a real system in USA, and composed by line regulator, transformer, unbalanced loads, and shunt capacitors.

Triphase AC/DC/AC inverter acts as PA. Its Active Front End (AFE) converter is connected to the Lab grid at 400 V/ 50Hz, this side of the PA has as main function the control of the internal DC bus voltage, which reference is stablished in 700 Vdc, by modifying active power flux. There is a DC link that allow the DC connections, this is used to interface with the DC side of HUT, as discussed next. The AC output acts as three-phase voltage source controlled by references sent by RTDS® through a FO link (Aurora protocol). A set of three variables controls PA output: Voltage RMS amplitude, frequency, and angle phase. The calculation time step of PA is 62.5 µs.

Triphase DC/AC inverter acts as HUT. Its DC side is connected to the DC link of PA, which has a nominal voltage reference of 700 Vdc. This connection represents an array of PV panels with the main difference that, in this case, the characteristic IV-curve is not being considered. At AC side, HUT is connected to PA voltage source output. HUT inverter has a current control loop, where the references are established by Simulink as HMI (Human Machine Interface) and

emulate the modification of PV generation levels.

Since both Triphase converters are controlled from the same Real Time Target (RTT), an Inter Process Communication loop is implemented to allow data sharing between both devices. In this test case 2, a pair of current references (I_d^{ref}, I_q^{ref}) are sent to HUT by the automatic FP control, that is implemented at RTDS®. I_d^{ref} is the direct axis current reference and oversees active power control. Since the current reference is initially established by HMI, as mentioned above, I_d^{ref} has a meaning of maximum current limit, that may be applied (as curtailment) to avoid voltage violations. I_q^{ref} is the quadrature axis current reference and oversees reactive power control. In this case, I_q^{ref} overlaps the reference settled in Simulink.

3.2.2 Software set-up

The IEEE 34 bus feeder was modeled at RSCAD FX 1.3.1 during the LA period. The default benchmark was modified to include the injection of PV generation at Bus 830, as schematically shown in Figure 4. This power injection corresponds to the one physically injected by HUT. Details about the interface between software and hardware environments are presented in Section 3.2.3. The model makes use of two RTDS® Novacor racks, with power system separation in two subsystems at Bus 854. The model is executed in real time with a timestep of 55 µs. It is worth to mention that the highlighted buses in Figure 4 are the ones monitored during the tests, in terms of rms voltage profile.

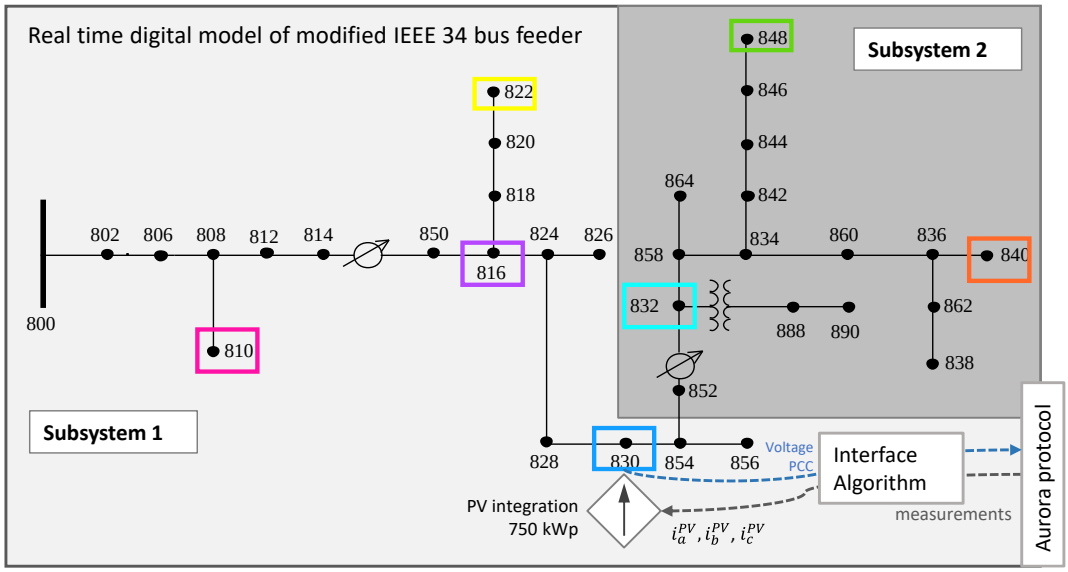

Figure 4: One-line diagram of modified IEEE 34 bus feeder.

Besides the electrical model itself, the programing made at RSCAD also include the algorithm interface, rms and waveform measurements, Aurora link configuration, plot update logic for triggered measurements, and the automatic PF control implementation.

The PF control implemented in RSCAD is presented by the flowchart of Figure 5. This loop is executed every 10 s and has the function of determining the current references to be sent digitally to HUT (I_d^{ref}, I_q^{ref}). It is observed that if the control is deactivated the references are 1 pu and 0 pu, respectively, with represents a unity PF. On the other side, there are three different behaviors in the case the control is activated, in function of the comparison between all the monitored rms voltages with two thresholds 1.05 pu (lim_1) and 1.03 pu (lim_2): i) if the

maximum voltage among the buses analyzed exceeds lim_1, then I_q^{ref} is adjusted to increase the reactive power absorption in 0.1 pu, in terms of the reactive power of the previous control loop execution; ii) if all the voltages are in $lim_2 < V < lim_1$ range, then the currents references remain constant; iii) if all the voltage are less than lim_2, then I_q^{ref} is adjusted to reduce the reactive power absorption in 0.1, which means that the consumption of reactive power, as an ancillary service, is no longer required.

It can be observed that I_q^{ref} is limited to a minimum value of -1 pu and a maximum value of 0, therefore this control only acts in the sense of avoid over-voltages. It is worth highlight that I_d^{ref} is calculated as the remaining active power capability to avoid over-loading of the PV inverter, which can lead to power curtailment.

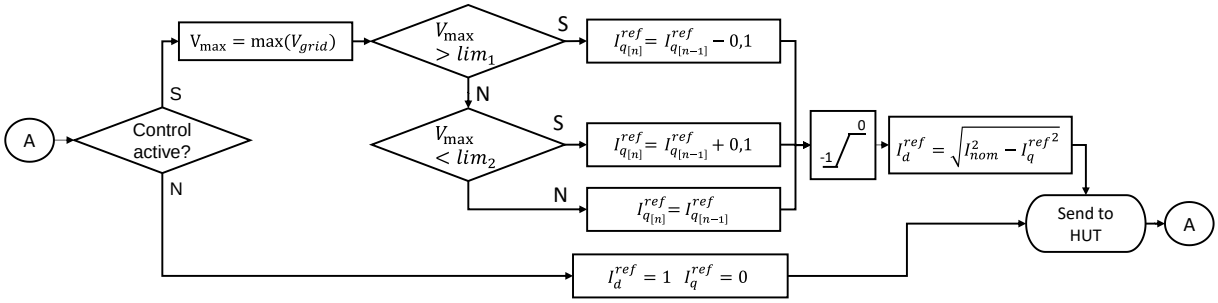

Figure 5: RSCAD implementation of the used automatic PF control.

Triphase-converters control functions

The developed PHIL test bench makes use of the original inner control loops of Triphase converters, which are based on a virtual circuit control theory (Hendrickx et al., 2016; Niyomsatian et al., 2017). Therefore, in respect of this work, the control of these converters is given by the definition of the input references.

In the case of PA converter, three input references are used: i) rms voltage magnitude (V_{rms}^{PCC}), ii) voltage frequency (F^{PCC}) and iii) voltage phase shift (θ^{PCC}). These references are calculated in the RDTS and sent to Triphase's RTT via Aurora link. Details about this implementation are presented in Section 3.2.3.

In the case of HUT converter, the input references are direct and quadrature currents (I_d^{PCC}, I_q^{PCC}) that are defined by the combination of HMI inputs refences (I_d^{IHM}, I_q^{IHM}) and the output of the PF control loop (I_d^{ref}, I_q^{ref}). The logic implemented is presented next.

If $I_d^{ref} \leq I_d^{HMI}$ Then $I_d^{PCC} = I_d^{HMI}$ Else $I_d^{PCC} = I_d^{ref}$ End	If $I_d^{ref} = 0$ Then $I_d^{PCC} = I_d^{HMI}$ Else $I_d^{PCC} = I_d^{ref}$ End

Taking advantage of both converters controls being implemented in the same RTT, a Circular Inter-Process Communication (CIPC) was performed to allow digital communication between both devices. CIPC is a shared memory strategy based on ring-buffers that allows Simulink models to share data in the same time step of model execution (62.5 µs).

3.2.3 Interface algorithm set-up

Interface algorithm is the denomination given to the software and hardware configuration performed to stablish the interconnection between digital (RTS) and real (PA and HUT) worlds. This

research makes use of a modified version of Ideal Transformer model (ITM) (Lauss et al., 2016), as described next.

From RTS to PA

As described above, the inputs of PA are the variables V_{rms}^{PCC}, F^{PCC} and θ^{PCC}, that are calculated by the real time model and sent to PA through Aurora optic link. This is implemented in RSCAD in the following manner:

- V_{rms}^{PCC} is calculated as the mean of phases A, B and C rms voltage measurements. Once the simulated nominal voltage differs of the real one at PA terminals (24,9 kV vs 380 V), a factor of 15.26 × 10^{-3} [V /V] is applied.
- F^{PCC} is constant in 60 Hz in this case study once the input source at Bus 800 is modelled as a voltage source behind a series impedance and not as machine models.
- θ^{PCC} is stablish as constant zero.

From PA to RTS

Current measurements of PA are sent back to RTS to close PHIL loop. Besides, Simulink model of PA includes a phase-locked-loop (PLL) to determinate fundamental magnitude and angle of HUT injected currents ($I_{HUT}^{PLL}, \theta^{PLL}$), which are the feedback variables for RDTS digital simulation model.

In RTS side, the signals are used to determinate the instantaneous references for a set of controlled source currents connected at Bus 830, as shown in Figure 6. Therefore, the real power measured at HUT terminals is proportionally represented at RTS simulation model. To represent a medium size distribution generation unit, 750 kW was defined as the nominal PV generation at real time model, which leads to the use of a conversion factor of 0.763 [A /A] and a power relationship between real power and simulated one of 50 [kW/kW]. As presented in the figure, a first-order filter, with cut-off frequency of 5 kHz, is applied at current magnitude to avoid oscillations.

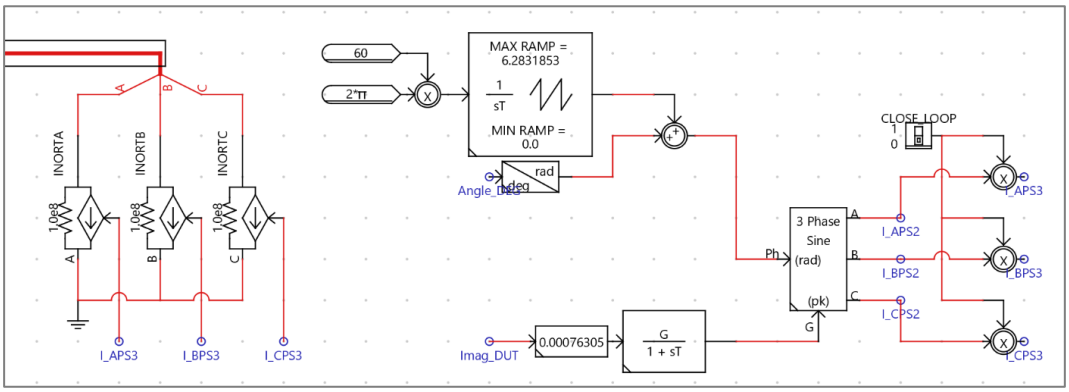

Figure 6: RSCAD implementation of feedback current injection

An important component of Figure 6 block programming is the binary input “close loop” that controls the moment the calculated feedback currents ($i_a^{PV}, i_b^{PV}, i_c^{PV}$) are effectively injected into RTS model, as depicted by the procedure presented in Section 3.1.2.

3.2.4 Main differences between PHIL test benches

Considering the set-up characterization of ESP Lab’s PHIL set-up, presented in the previous

three Sections, the main differences between this set-up and the one developed at CEPEL's lab are presented next.

Hardware set-up

The PHIL test bench developed at CEPEL's lab as part of the current research is composed by an OPAL-RT® RTS, a Spitzenberger & Spies linear amplifier as PA, and a Triphase programable inverter as HUT, Figure 7 shows a schematic diagram of the hardware set-up.

In this research the digital model implemented in both PHIL set-ups is the same, so the difference between the systems relies in the use of distinct device brands. CEPEL's RTS model is executed with a time step of 40 µs.

Regarding PAs, linear and switched amplifiers have different operation principles and performance characteristics, as described in (Brandl, 2017). Besides, in CEPEL's PHIL test bench the references sent from RTDS to PA, as well via Aurora protocol, are the instantaneous phase voltage references $(v^*_{PCCa}, v^*_{PCCb}, v^*_{PCCc})$, instead of phasor quantities. Additionally, in contrast with ESP Lab's PA, CEPEL's does not have an available DC link to connect with.

CEPEL's Triphase HUT has similar specifications that ESP Lab's. The two main differences between them are: i) CEPEL's Triphase is a four-wire equipment (ESP Lab's HUT is a three-wire equipment), what allows unbalance current injection; ii) CEPEL's Triphase has an additional DC/DC internal converter. Therefore, the configuration of CEPEL's Triphase is DC/DC-DC/AC versus just DC/AC in ESP Lab's case. Furthermore, CEPEL´s HUT does not have an available DC link connection, neither Aurora link communication.

CEPEL's PHIL set-up requires the use of and additional DC source, connected at DC HUT terminals. A Regatron GSS series source with constant voltage reference of 550 V is used.

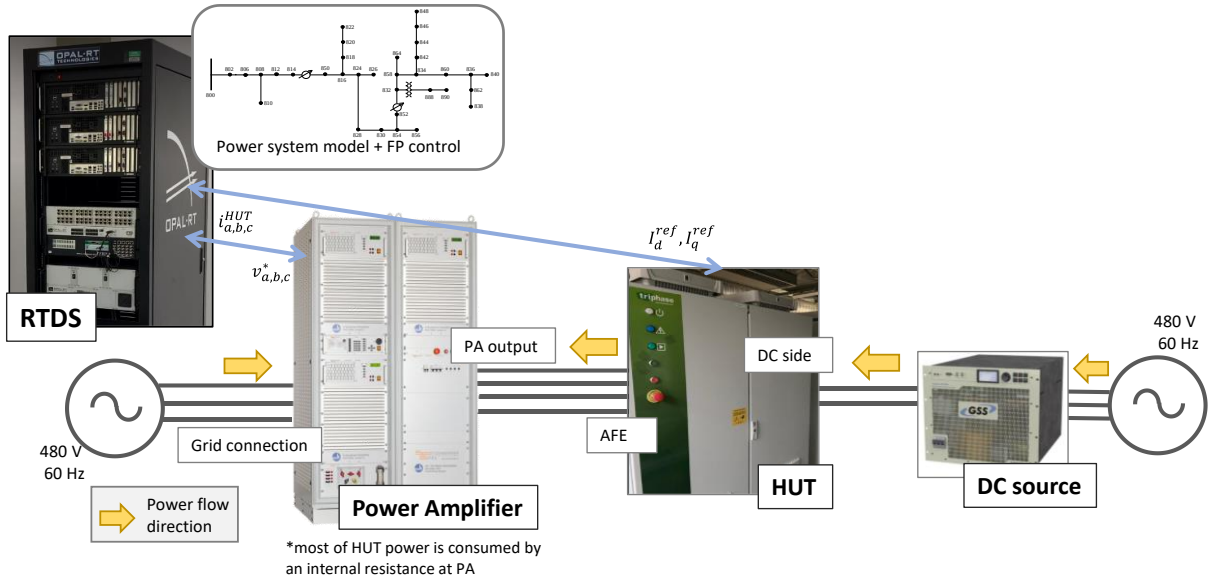

Figure 7: Schematic diagram of Hardware set-up at Lab SG.

Software set-up

The configurations and programming shown in Section 3.2.2, including IEEE 34-bus feeder and FP control were also implemented in OPAL-RT simulator, using Simulink and RT Lab environments. The simulation time step is stablished at 40 µs.

It is worth highlight that at the beginning of LA Period, CEPEL's PHIL test bench did not count with digital communication interface between HUT and RTDS, and that CEPEL's Triphase

devices does not have Aurora communication feature. Therefore, to allow the execution of test case 2 at CEPEL's lab, a Modbus TCP implementation were performed between OPAL-RT and Triphase after finishing the LA Period. Even though Modbus is not a real time protocol, it was selected for this application because of its worldwide acceptance (which can lead to future inclusion of third-party devices into PHIL test bench) and in view of I_d^{ref} and I_q^{ref} being variables with slow dynamics, as the implemented FP control is. Figure 8 represents the communication-links differences between both PHIL test benches.

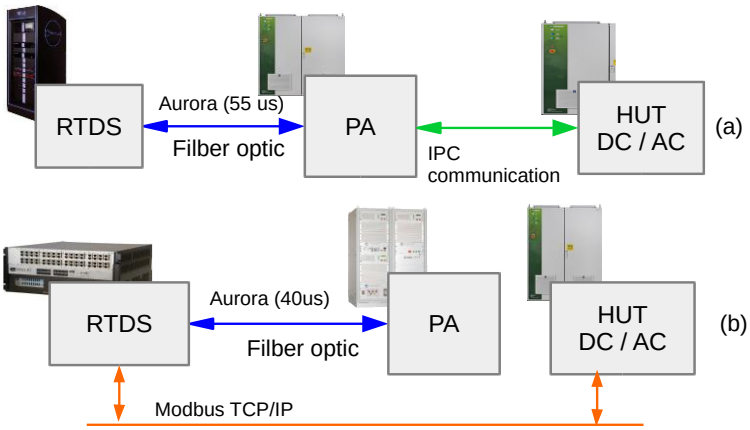

Figure 8: Communication links at PHIL test benches: (a) ESP's Lab set-up; (b) CEPEL's lab set-up.

Interface Algorithm set-up

As done in ESP Lab's case, ITM with proportionally gains adjustments is used as interface algorithm, however, given the use of a linear amplifier, the implementation differs, as presented next:

From RTS to PA

In this case, the inputs of PA are the instantaneous variables v_a^*, v_b^* and v_c^*, that are the direct results of voltage measurement at RTDS, with the 15.26 × 10^{-3} [V /V] conversion factor applied.

From PA to RTS

Instantaneous current measurements of PA ($i_a^{HUT}, i_b^{HUT}, i_c^{HUT}$) are sent back to RTDS through Aurora link. The conversion factor of 0.763 [A /A] is applied. Additionally, a first order filter with cut-off frequency of 900 Hz[1] is introduced to obtain the references for the current controlled sources ($i_{a,b,c}^{PV}$).

Table 3 presents a summary of the most relevant differences between both PHIL test benches. These aspects have potential impacts on replicability achievement.

Table 3: Summary of main differences between PHIL test benches for replicability evaluation

PHIL component	ESP Lab	CEPEL Lab
Hardware	Switched type power amplifier	Linear type power amplifier
	Three-wires DC/AC HUT	Four-wires DC/DC-DC/AC HUT
	DC connection between HUT and PA	Use of additional DC source connected at HUT's DC terminals
Interface algorithm	RMS (magnitude and phase) voltage and	Instantaneous voltage and current

[1] This setting was recommended by researchers of the Institute of Communication and Computer Systems (ICCS) of National Technical University of Athens (NTUA), in a virtual meeting during LA period.

	current references and PLL	references
Communication	Aurora and CIPC links	Aurora and Modbus links

3.3 Data Management and Processing

Both virtual variables and electrical measurements are processing by RTS in each PHIL test bench. On the one hand, voltage and currents waveforms at PCC are measured by PAs and send back to RTS. On the other hand, voltage profiles over the entire feeder, power calculations and binary variables are computed in RTDS itself.

At ESP Lab's PHIL set-up, the measurements of interest are exported as .csv format. A Matlab script, available in Appendix A, is used to plot the results, that are also saved as .emf format. At CEPEL's PHIL set-up, results are automatically saved as .mat format accordingly with the operation of the respective trigged. All the data is available at a Microsoft OneDrive repository. As shown in Appendix A, further mathematical operations are performed at Matlab in both cases.

As presented in Section 4.1, point-to-point waveform comparisons between the couple of results is not suitable. Therefore, the replicability analysis is performing by qualitatively comparison.

4 Results and Conclusions

4.1 Discussion of Results

The variables shown in the analysis presented in this Section are: i) PV current injection, ii) PV virtual power injection, iii) voltage profiles over the selected buses of IEEE 34 bus feeder.

4.1.1 Test case 1 – unity power factor power injection

Results at ESP Lab

Figure 9 shows the dynamics of current injection increase at PCC accordingly with the step vii) of the procedure shown in Section 3.1.2. A fast and not oscillating current control can be observed, as the currents reach its reference in about 20 ms. The instantaneous active and reactive powers (Akagi et al., 2007) caused by this power injection are shown in Figure 10, a virtual power of about 745 kW with PF close to unity is reached at B830.

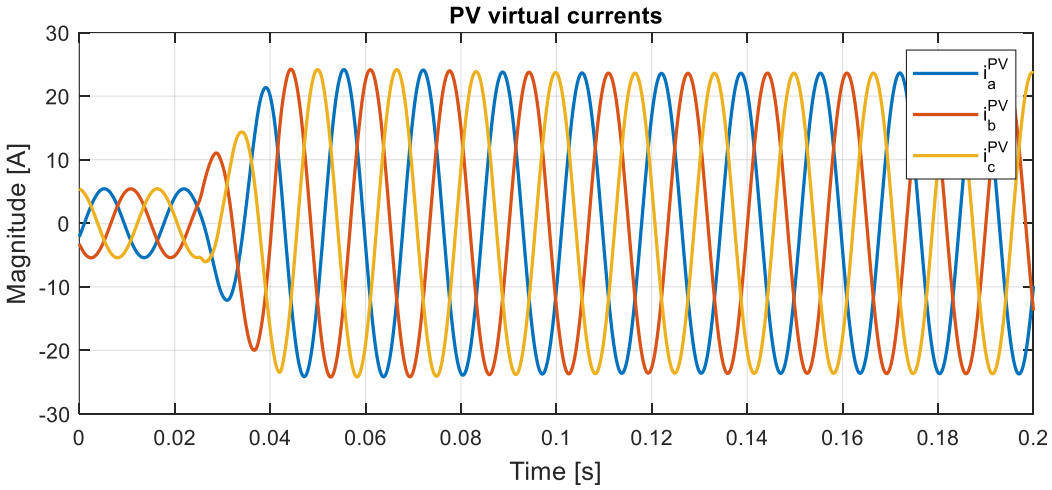

Figure 9: HUT current increase dynamics (step vii of Section 3.1.2 procedure)- ESP Lab.

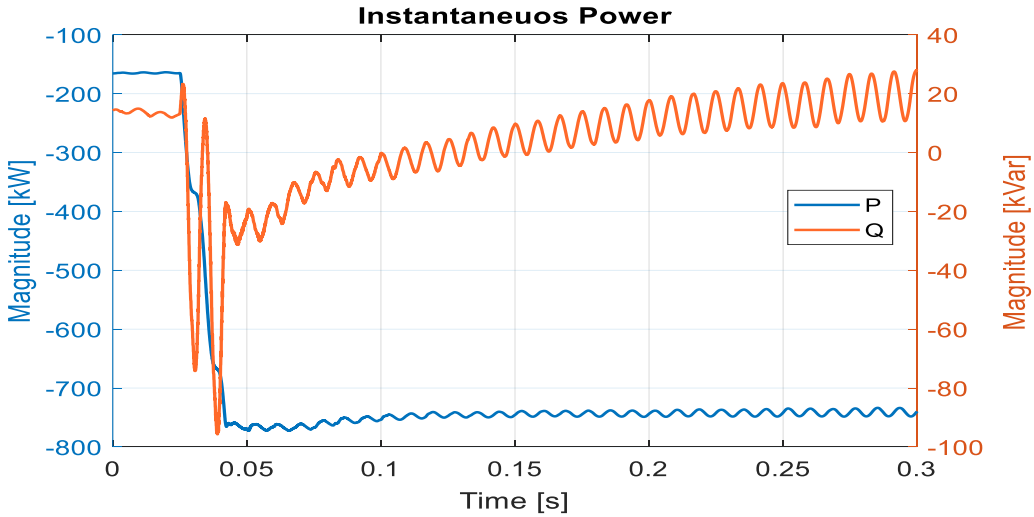

Figure 10: Virtual PV power injection due to HUT current increase- ESP Lab.

As expected, the unity PF power injection originates voltage variations over the entire benchmark feeder, behavior shown in Figure 11. It can be observed that for some buses the voltage amplitude exceeded PRODIST Adequate limits. It is worth highlighting that Bus 830 is still operating with a voltage level lower than the 1.05 pu threshold, which means that a local control loop, implemented at PV inverter based on PCC measurements, would not be able to identify this anomaly by itself, raising the importance of centralized or distributed control loops to achieve higher levels of DG hosting capability.

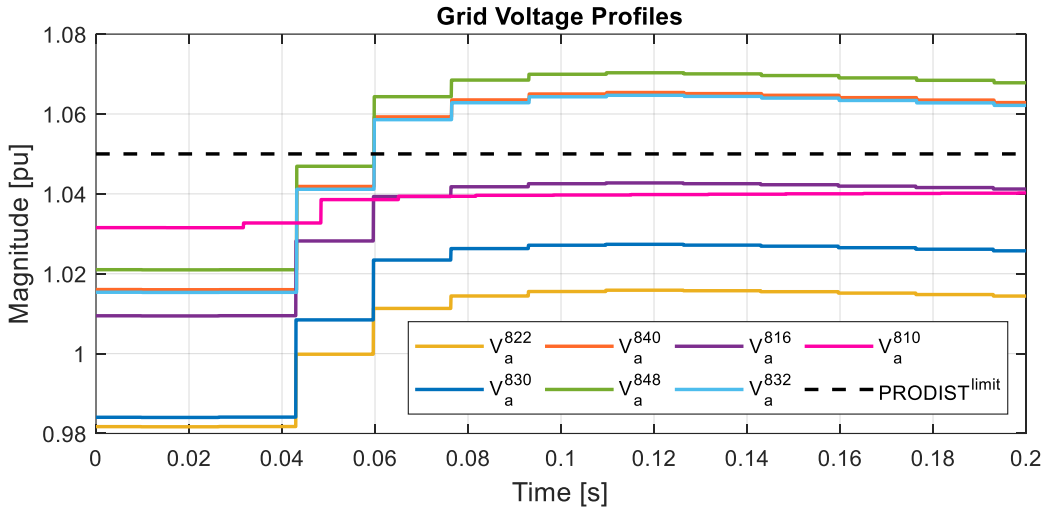

Figure 11: Voltage profiles for test case 1- ESP Lab.

Results at CEPEL Lab

The dynamic current behavior obtained at CEPEL test bench is shown in Figure 12.Clearly, the control loop settings of this HUT are different from the ones at ESP Lab, once the currents dynamics show an under-damped response with overshoot and short setting time. However, the steady state currents are comparable with the ones obtained at ESP Lab (Figure 9), taking into consideration that CEPEL's HUT allows the injection of unbalanced three-phase currents.

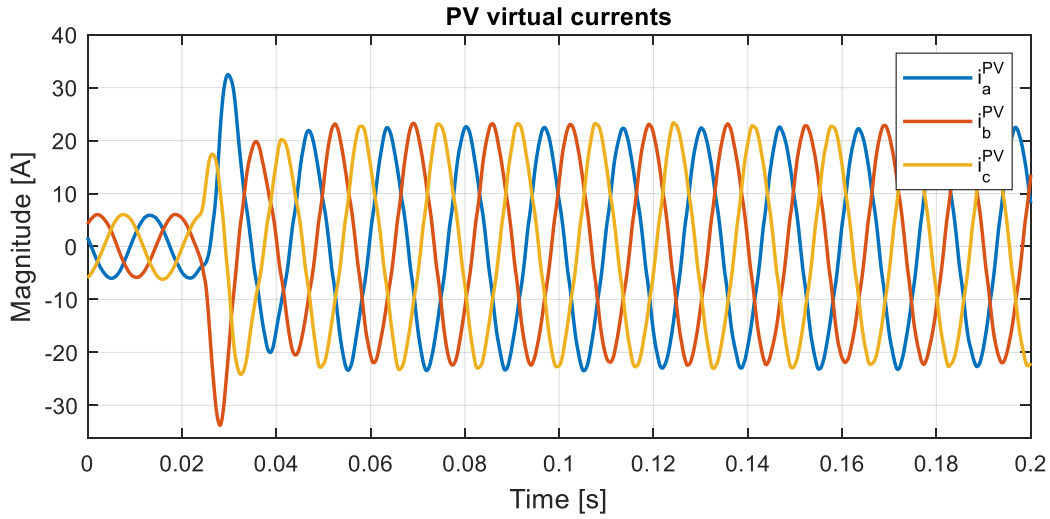

Figure 12: HUT current increase dynamics (step vii of Section 3.1.2 procedure)- CEPEL Lab.

Instantaneous active and reactive powers are shown in Figure 13. A fast dynamic is observed as *P(t)* reaches about 750 kW in less than 20 ms, with an overshoot that exceeded 1000 kW. As presented, there is coupling between active and reactive power, which leads to reactive

power injection in this operation mode. This operation, which is not ideal, could be explaining by an inappropriate internal HUT PLL performance due the unbalanced voltages present at HUT terminals (Figure 14). It is worth highlighting that in ESP Lab case PCC voltages are balanced due the limitations of the PHIL PA. As discussed before, the modification of HUT internal control loops is not within the scope of the current research.

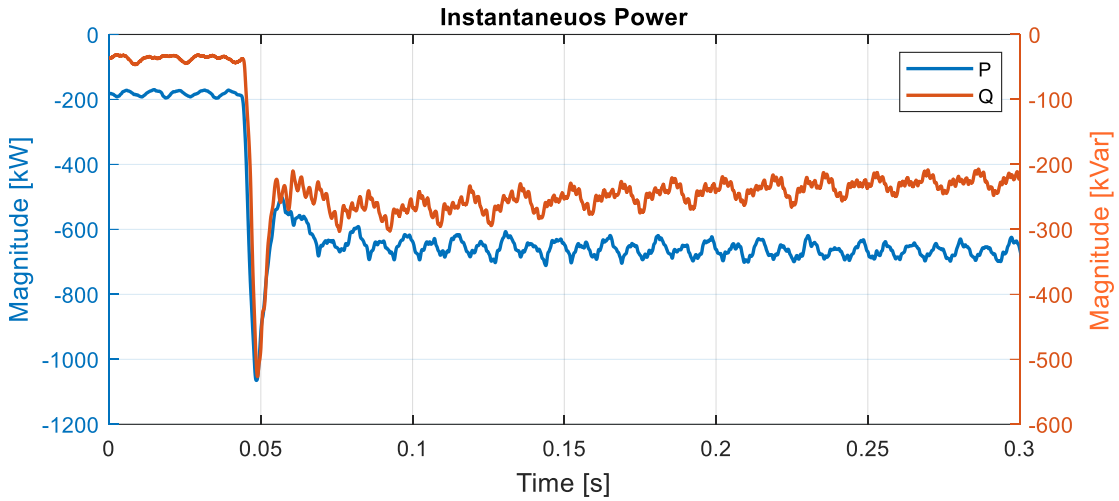

Figure 13: Virtual PV power injection due to HUT current increase- CEPEL Lab.

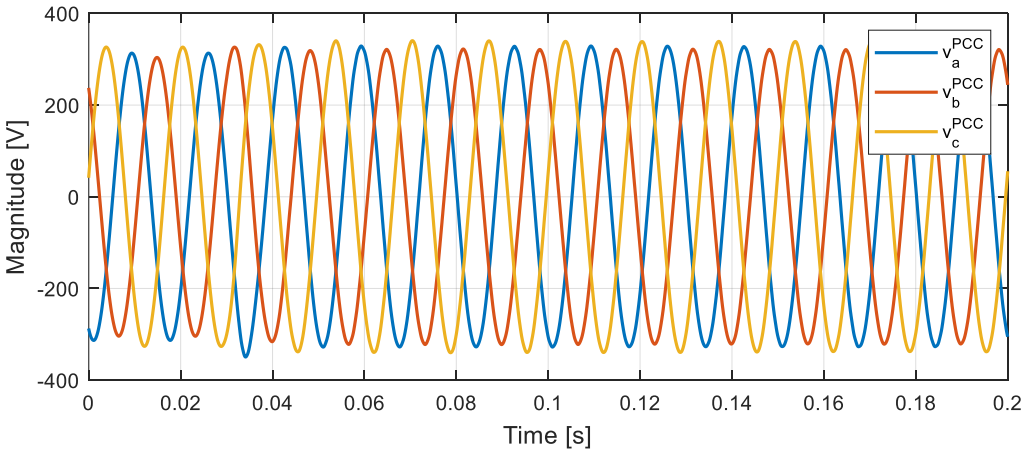

Figure 14: Voltage at HUT terminals- CEPEL Lab.

Voltage profiles over IEEE 34 bus feeder for CEPEL Lab's case are shown in Figure 15. As it happened at ESP Lab test bench, the power injection causes over voltage violations. In this case, some of the buses exceeded the 1.05 pu threshold, which can be justified by the injection of reactive power, as shown previously.

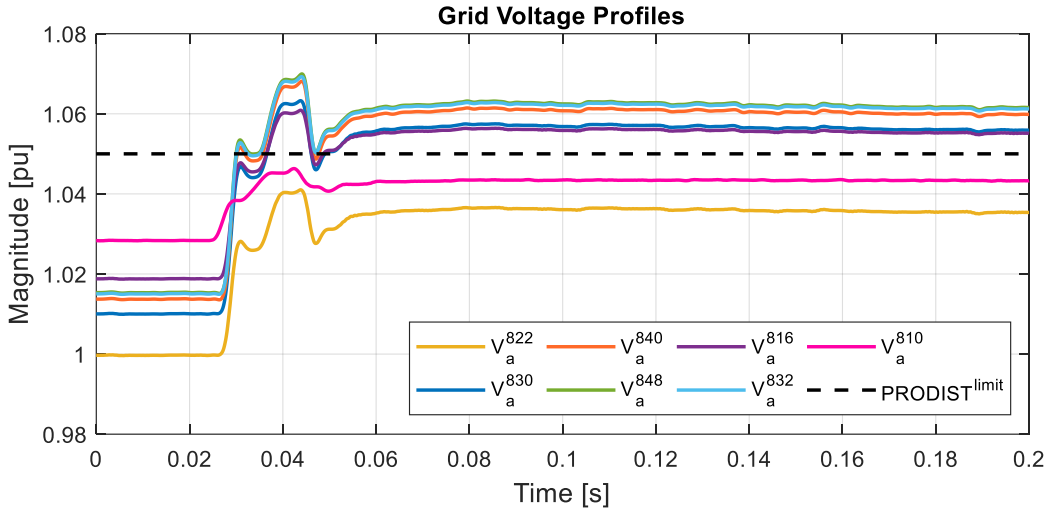

Figure 15: Voltage profiles for test case 1- CEPEL Lab.

4.1.2 Test case 2 – application of PF controller

The following results correspond to the activation of the automatic PF control, item viii of the procedure presented at Section 3.1.2.

Results at ESP Lab

The experimental results for test case 2 testing at ESP Lab are presented by Figure 16 (currents injected at PCC), Figure 17 (instantaneous active and reactive power) and Figure 18 (rms grid profile over the selected points of the feeder). As shown, the PF controls modifies the reactive power to successfully bring back the voltage levels to the ones accepted by Brazilian quality distribution grid quality standard.

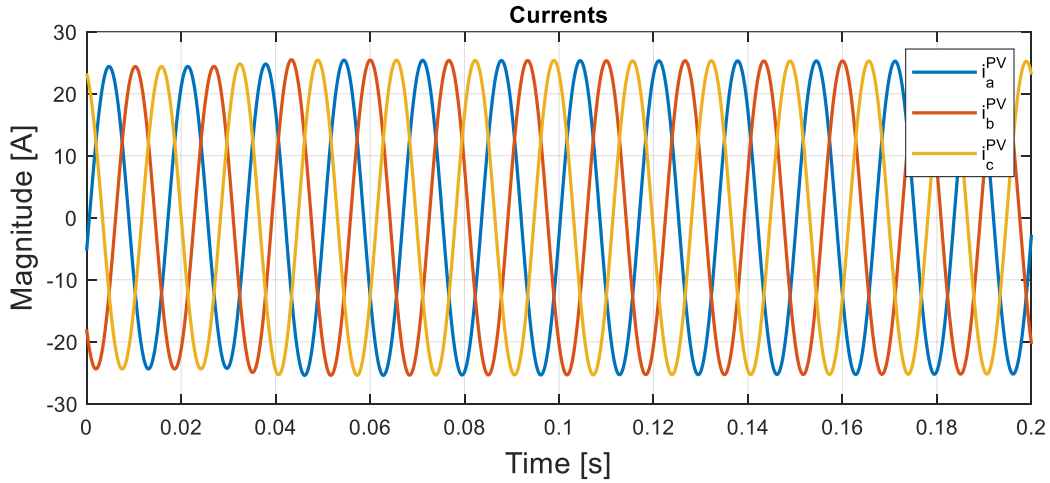

Figure 16: HUT current dynamics for automatic PF control – ESP Lab.

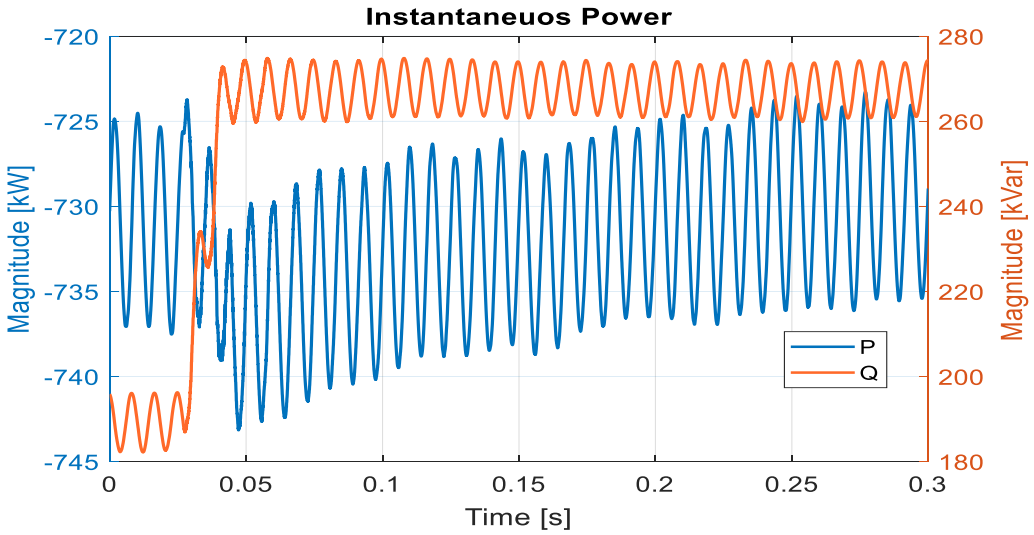

Figure 17: Virtual PV power injection due to FP control- ESP Lab.

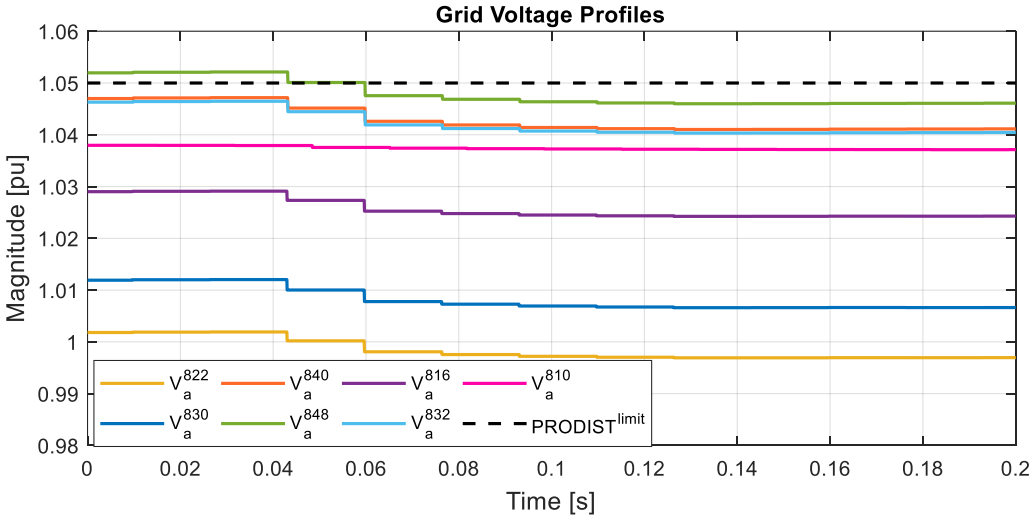

Figure 18: Voltage profiles for test case 2- ESP Lab.

Results at CEPEL Lab

Following the same sequence for results presentation, Figure 19, Figure 20 and Figure 21 presents experimental test case 2 outcomes at CEPEL lab. It is observed that the overall goal of reducing rms voltage levels under 1.05 pu threshold is achieved. In this case, however, the reactive power reference stablished by PF control is bigger, leading to more severe voltage reductions and more evident current increments.

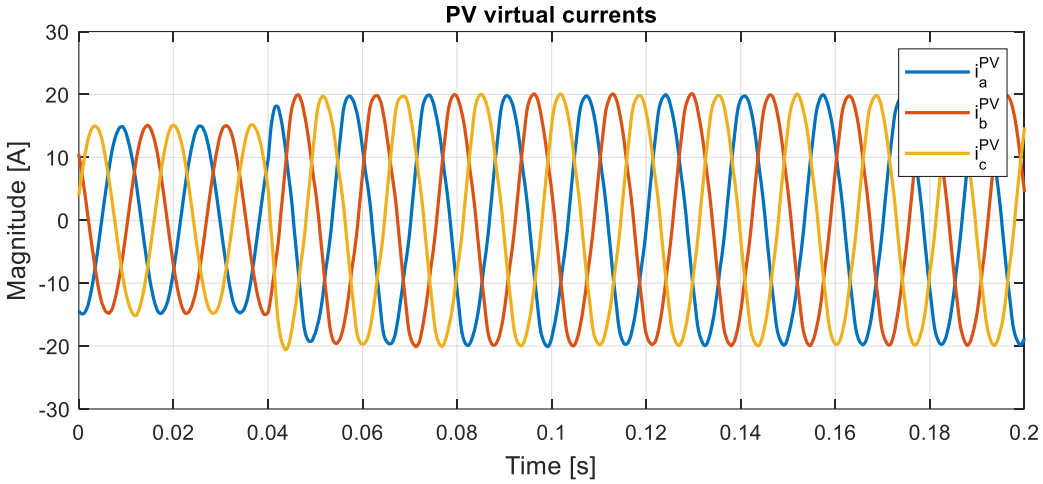

Figure 19: HUT current dynamics for automatic PF control – CEPEL Lab.

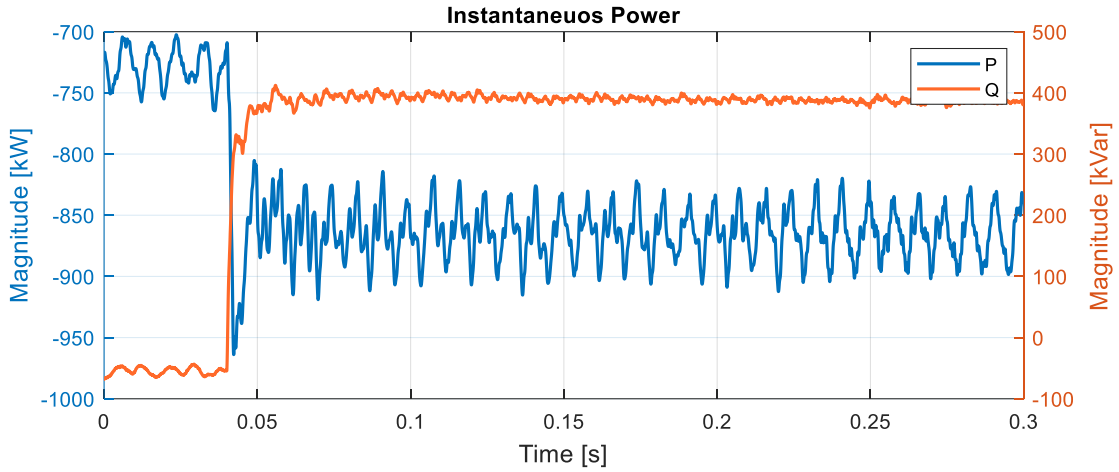

Figure 20: Virtual PV power injection due to FP control- CEPEL Lab.

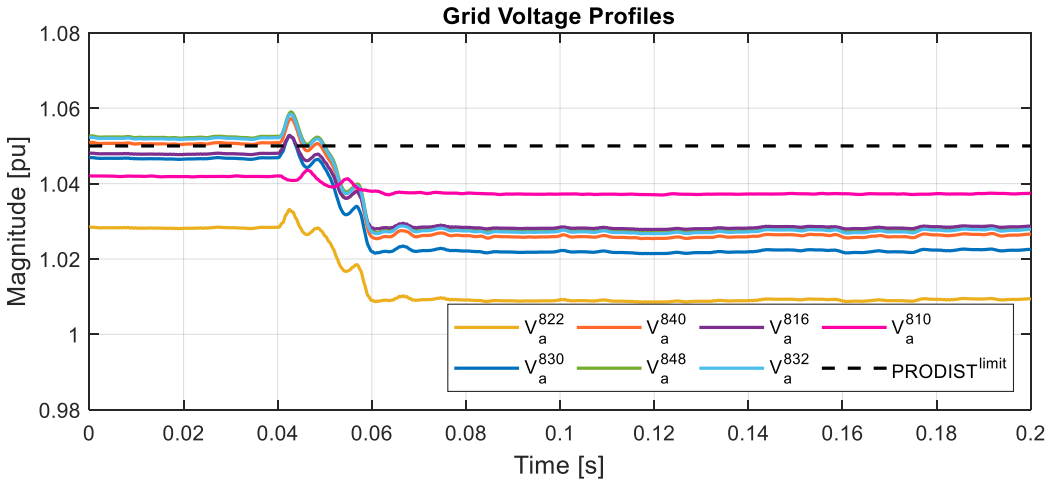

Figure 21: Voltage profiles for test case 2- CEPEL Lab.

4.1.3 Discussion

Both test benches were able to represent the voltage/medium power PV injection issue satisfactorily, in the sense that in both cases it was possible to observe voltage violations as

consequence of unity power factor DG insertion, and to verify the suitable use of a simple ancillary service (PF control, for example) as a tool to avoid those voltage violations. From this point of view, these results lead to understand that CEPEL Lab's PHIL test bench was successfully replicated at ESP Lab infrastructure, although there are relevant components differences.

It is worth highlight that waveform comparisons between the set of results it is not reasonable because of the differences between both set-ups, as presented in Section 3.2.4. For instance, ESP Lab's PA is not able to create unbalance voltage waveforms, therefore this characteristic of IEEE 34 bus feeder is not within the representation scope at ESP Lab, however it was represented at CEPEL Lab.

4.2 Conclusions

As result of this LA, an adaptation of CEPEL's PHIL test bench was established at hosting infrastructure, using its local resources. Although ESP Lab's PHIL set-up significatively differs from the one developed at CEPEL Lab, both set of experimental results lead to the same conclusion regarding PV hosting capability levels due to overvoltage issues. Additionally, the implemented PF control loop proved to be appropriate, for the modeled grid, to avoid overvoltage deviations, in both set-ups. Therefore, from a high-level perspective, PHIL replicability was confirmed for the current case study.

On the other hand, the set of results highly differ between them from a waveform comparison level. This is caused by the several differences between both PHIL set-ups, among them the more relevant are: i) four-wire hardware equipment (CEPEL) vs three-wire hardware equipment (ESP Lab), ii) interface algorithm based on instantaneous variables (CEPEL) vs interface algorithm with rms quantities (ESP Lab) and iii) non-real time MODBUS communication for PF control setpoint establishment (CEPEL) vs Aurora real time communication (ESP Lab). To reduce waveform discrepancies, it is recommended, for future multi-lab PHIL comparisons, to use the same interface algorithm and number of active wires in both set-ups.

It was identified that the Interface Algorithm definition is the factor that influence more representative in obtaining a comparable case study using different RTDS/HIL infrastructures.

Otherwise, the LA program considerably improved the technical competences of User Group team regarding PHIL simulation area. The LA period provided insights for test refinements, specifically regarding the introduction of automatic PF control via a communication protocol, which is in accordance with the holistic test procedure for system validation presented at (T. I. Strasser et al., 2020). This improvement opens the door to the introduction of third-party devices into PHIL set-up, like commercial DG controllers. Additionally, the LA program created a collaboration tie between both institutions, with potential benefits for both.

5 Open Issues and Suggestions for Improvements

The following improvement are suggested:

- To perform a study whereas the electrical model represented at the RTS does not include unbalanced voltages and currents.
- To modify the internal Triphase converter controllers to have the same set of adjustments in both PHIL set-ups
- Since the establishment of PHIL set-up at ESP Lab took a relevant part of LA period, it is suggested, for future similar projects, to create a methodology of local support from hosting-lab staff in such a way that a basic version of PHIL set-up will be ready at the beginning of LA.

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Appendix A

A.1. Screen captures of PHIL test benches HMIs

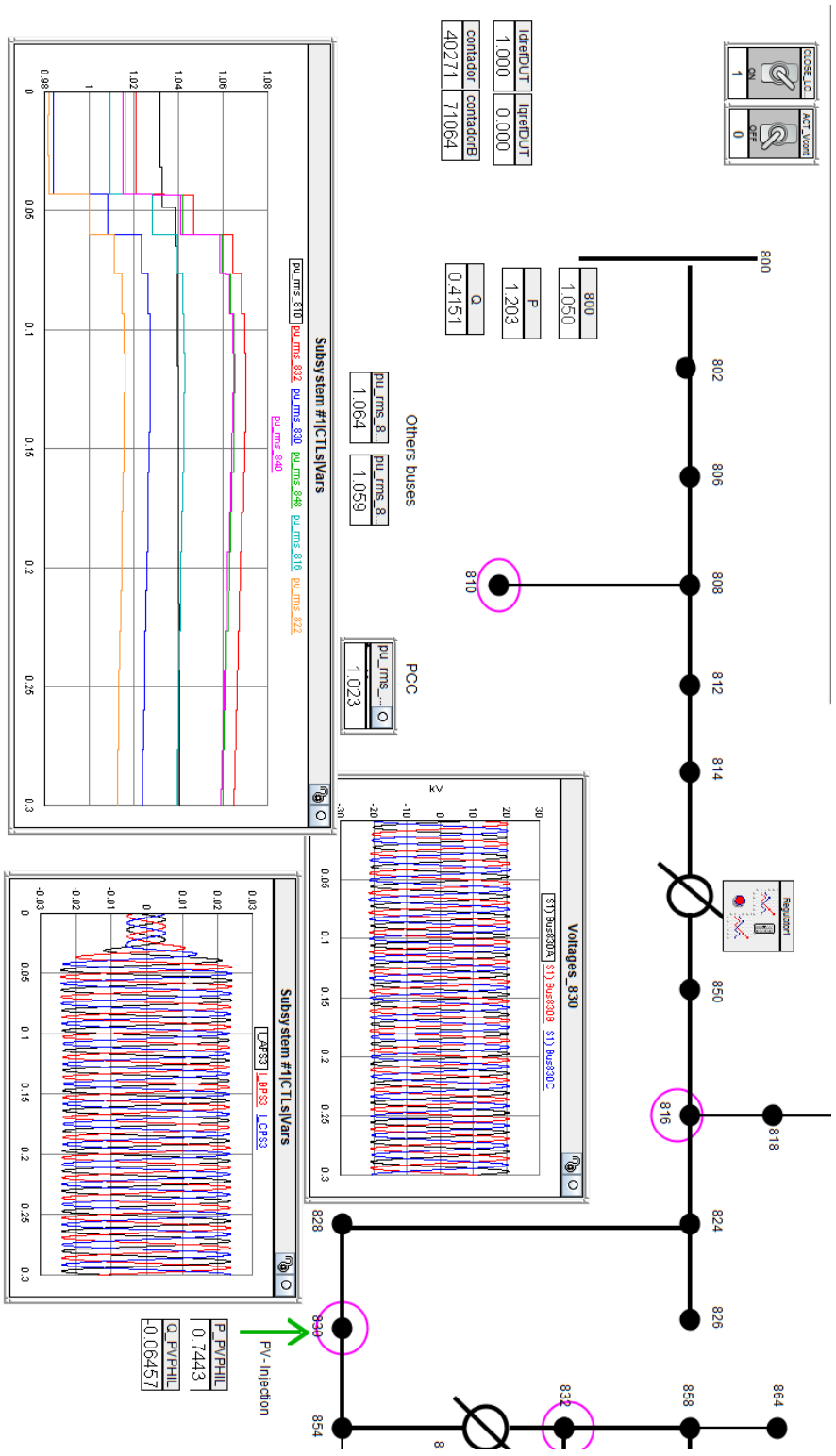

Figure A. 1: RSCAD HMI – ESP Lab.

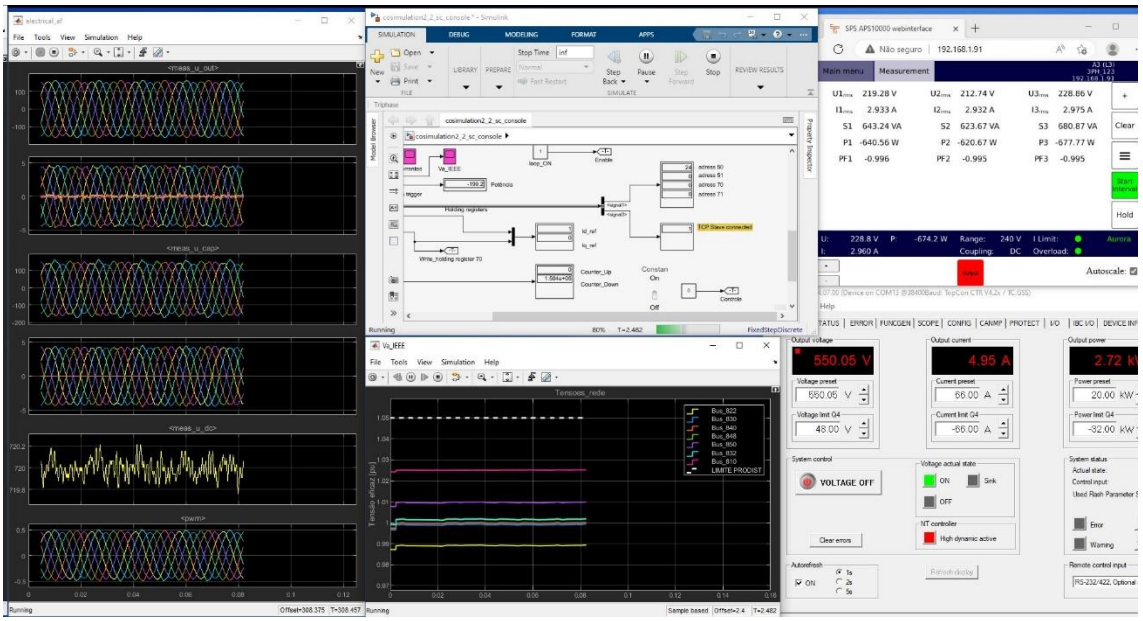

Figure A. 2: CEPEL Lab HMI (i) - Simulink (STR), web interface – (PA) and Topcontrol software – DC source.

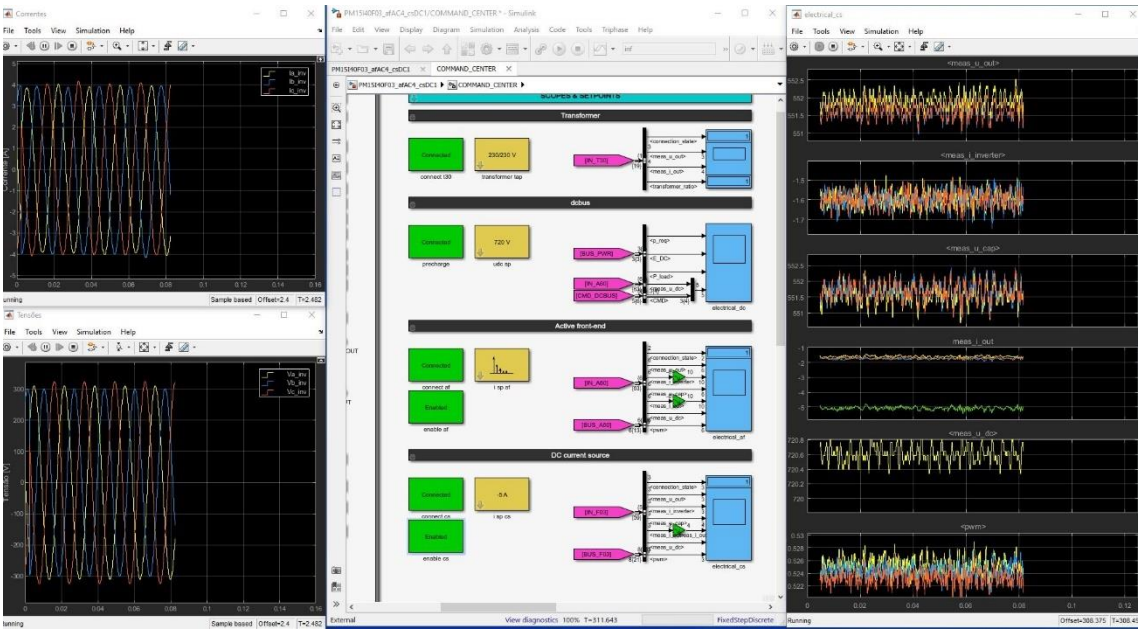

Figure A. 3: CEPEL Lab HMI (ii) - Simulink (HUT).

A.2. Matlab® script for data management

```
%% Open file
local = uigetfile();
arquivo = load(local);


prompt = {'Arquivo Group 1 = Subida //// Group 2 = Descida'};
dlgtitle = 'Seleção dos resultados (Subida (1) ou Descida (2))';
dims = [1 120];
definput = {''};
answer = inputdlg(prompt,dlgtitle,dims,definput);
aaa = str2double(answer);
tinicial =0.1;
tfinal = 0.5;

if aaa == 2
%% Plot Tensões Rede
figure('Renderer', 'painters', 'Position', [100 70 750 300]);
%plot de todas as variaveis direto
%plot(arquivo.data(:,[5:12])); %

%plot por par (tempo, var1, tempo, var 2...)
tempo= arquivo.data(:,1) - arquivo.data(1,1);
plot(tempo,       arquivo.data(:,5),tempo,       arquivo.data(:,6),tempo,       ar-
quivo.data(:,7),tempo,   arquivo.data(:,8),tempo,   arquivo.data(:,9),tempo,   ar-
quivo.data(:,10),tempo, arquivo.data(:,11),'linewidth', 1.5);
hold on
plot(tempo, arquivo.data(:,15),'k--','linewidth', 1.5);
hold off
xlim([tinicial tfinal]);
ylim([0.98 1.08]);
grid on
title('Grid Voltage Profiles');
legend('V_a822', 'V_a830', 'V_a840','V_a848', 'V_a816', 'V_a832','V_a810','PRODIST
Limit');
xlabel('Time [s]', 'Fontsize', 14);
ylabel('Magnitude [pu]', 'Fontsize', 14);

%% Plot Correntes


figure('Renderer', 'painters', 'Position', [100 200 750 300]);
plot(tempo,      arquivo.data(:,12),tempo,      arquivo.data(:,13),tempo,      ar-
quivo.data(:,14),'linewidth', 1.5); %12 a 14 versao + atual
xlim([tinicial tfinal]);
title('Currents');
grid
legend('i_{a}^{PV}', 'i_{b}^{PV}', 'i_{c}^{PV}');
xlabel('Time [s]', 'Fontsize', 14);
ylabel('Magnitude [A]', 'Fontsize', 14);


%% Plot Pativa
figure('Renderer', 'painters', 'Position', [100 400 750 300]);
plot(tempo, arquivo.data(:,4),'linewidth', 1.5);
xlim([tinicial tfinal]);
title ('Active Power');
legend('Pactive');
grid on
xlabel('Time [s]', 'Fontsize', 14);
ylabel('Magnitude [W]', 'Fontsize', 14);

%% Plot potencia usando potÊncia instantanea - PQ
figure('Renderer', 'painters', 'Position', [100 200 750 300]);
    I_830 = arquivo.data(:,12:14);
```

```
    V_830 = arquivo.data(:,16:18);
    Valfab=sqrt(2/3)*[1/sqrt(2)  1/sqrt(2)  1/sqrt(2); 1  -0.5  -0.5; 0  sqrt(3)/2  -
sqrt(3)/2]*V_830';
    ialfab=sqrt(2/3)*[1/sqrt(2)  1/sqrt(2)  1/sqrt(2); 1  -0.5  -0.5; 0  sqrt(3)/2  -
sqrt(3)/2]*I_830';
 %matriz PQ
    P = (Valfab(2,:).*(ialfab(2,:)) + Valfab(3,:).*(ialfab(3,:)))/10;
    Q = (Valfab(3,:).*(ialfab(2,:)) - Valfab(2,:).*(ialfab(3,:)))/10;
    yyaxis left
    plot(tempo, P(1,:),'b', 'linewidth', 1.5);
    ylabel ('Magnitude [kW]','Fontsize', 14);
    yyaxis right
    plot(tempo, Q(1,:),'r','linewidth', 1.5)
    ylabel ('Magnitude [kVar]', 'Fontsize', 14);
    grid on;
title('Instantaneuos Power');
legend('P', 'Q');
xlabel('Time [s]', 'Fontsize', 14);

%%clear temporary variables
clear local

else
figure('Renderer', 'painters', 'Position', [100 70 700 300]);
%plot de todas as variaveis direto
%plot(arquivo.data(:,[5:12])); %colocar 15 antes e de 5 a 11  versao + atual
%plot por par (tempo, var1, tempo, var 2...)
tempo= arquivo.data(:,1) - arquivo.data(1,1);
plot(tempo,      arquivo.data(:,13),tempo,      arquivo.data(:,15),tempo,      ar-
quivo.data(:,17),tempo,  arquivo.data(:,18),tempo,  arquivo.data(:,19),tempo,  ar-
quivo.data(:,20),tempo, arquivo.data(:,21),'linewidth', 1.5);
hold on
plot(tempo, arquivo.data(:,25),'k--','linewidth', 1.5);
hold off
xlim([tinicial tfinal]);
ylim([1 1.08]);
grid on
title('Grid Voltage Profiles');
legend('V_a822', 'V_a830', 'V_a840','V_a848', 'V_a816', 'V_a832','V_a810','PRODIST
Limit');
xlabel('Time [s]', 'Fontsize', 14);
ylabel('Magnitude [pu]', 'Fontsize', 14);

%% Plot Correntes
figure('Renderer', 'painters', 'Position', [100 400 700 300]);
plot(tempo,      arquivo.data(:,22),tempo,      arquivo.data(:,23),tempo,      ar-
quivo.data(:,24),'linewidth', 1.5);
xlim([tinicial tfinal]);
grid on
title('Currents');
legend('i_{a}^{PV}', 'i_{b}^{PV}', 'i_{c}^{PV}');
xlabel('Time [s]', 'Fontsize', 14);
ylabel('Magnitude [A]', 'Fontsize', 14);

%% Plot tensões rede


figure('Renderer', 'painters', 'Position', [100 200 750 300]);
plot(tempo,       arquivo.data(:,3),tempo,       arquivo.data(:,4),tempo,       ar-
quivo.data(:,5),'linewidth', 1.5);
xlim([tinicial tfinal]);
grid
legend('v_{a}^{PCC}', 'v_{b}^{PCC}', 'v_{c}^{PCC}');
xlabel('Time [s]', 'Fontsize', 12);
ylabel('Magnitude [V]', 'Fontsize', 12);

%% Plot Pativa
```

```
figure('Renderer', 'painters', 'Position', [100 700 700 300]);
plot(tempo, arquivo.data(:,27),'linewidth', 1.5);
xlim([tinicial tfinal]);
title ('Active Power');
legend('Pactive');
xlabel('Time [s]', 'Fontsize', 14);
ylabel('Magnitude [W]', 'Fontsize', 14);

%% Plot potencia usando potÊncia instantanea - PQ
figure('Renderer', 'painters', 'Position', [100 700 700 300]);
    I_830 = arquivo.data(:,22:24);
    V_830 = arquivo.data(:,3:5);
    Valfab=sqrt(2/3)*[1/sqrt(2) 1/sqrt(2) 1/sqrt(2); 1 -0.5 -0.5; 0 sqrt(3)/2 -
sqrt(3)/2]*V_830';
    ialfab=sqrt(2/3)*[1/sqrt(2) 1/sqrt(2) 1/sqrt(2); 1 -0.5 -0.5; 0 sqrt(3)/2 -
sqrt(3)/2]*I_830';
 %matriz PQ
    P = (Valfab(2,:).*(ialfab(2,:)) + Valfab(3,:).*(ialfab(3,:)))/10;
    Q = (Valfab(3,:).*(ialfab(2,:)) - Valfab(2,:).*(ialfab(3,:)))/10;
    yyaxis left
    plot(tempo, P(1,:),'b', 'linewidth', 1.5);
    ylabel ('Magnitude [kW]','Fontsize', 14);
    yyaxis right
    plot(tempo, Q(1,:),'r','linewidth', 1.5)
    ylabel ('Magnitude [kVar]', 'Fontsize', 14);
    grid on;
title('Instantaneuos Power');
legend('P', 'Q');
xlabel('Time [s]', 'Fontsize', 14);

%%clear temporary variables
clear local
end
```

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