



European Research Infrastructure supporting Smart Grid and Smart Energy Systems Research, Technology Development, Validation and Roll Out – Second Edition

Project Acronym: **ERIGrid 2.0**

Project Number: **870620**

Technical Report Lab Access User Project

Advanced GPT Inverter Physical Demonstration (AGIPDem [135])

Access Duration: 12-13/04/2023 to 05/05/2023

Additional remote tests: 15-17/08/2023

Funding Instrument: Research and Innovation Action
Call: H2020-INFRAIA-2019-1
Call Topic: INFRAIA-01-2018-2019 Integrating Activities for Advanced Communities

Project Start: 1 April 2020
Project Duration: 54 months

User Group Leader: C. T. Gaunt (University of Cape Town, South Africa)



Report Information

Document Administrative Information	
Project Acronym:	ERIGrid 2.0
Project Number:	870620
Access Project Number:	135
Access Project Acronym:	AGIPDEM
Access Project Name:	Advanced GPT Inverter Physical Demonstration
User Group Leader:	Charles Trevor Gaunt (University of Cape Town, South Africa)
Document Identifier:	ERIGrid2-Report-Lab-Access-User-Project-AGIPDEM-draft-vn.3
Report Version:	vn.3.0
Contractual Date:	dd/mm/yyyy
Report Submission Date:	dd/mm/yyyy
Lead Author(s):	CT Gaunt (UCT), P Jankee (UCT)
Co-author(s):	G Burt (University of Strathclyde), Z Feng (University of Strathclyde), R Munro (University of Strathclyde), I Abdulhadi (University of Strathclyde), B Feizifar (University of Strathclyde), M Malengret (UCT)
Keywords:	General Power Theory, Inverters, PHIL, Real-lab test, European Union (EU), H2020, Project, ERIGrid 2.0, GA 870620
Status:	x draft, final

Change Log

Date	Version	Author/Editor	Summary of Changes Made
24/07/2023	v1.0	Jankee/Gaunt (UCT)	First draft of report
28/10/2023	V2.0	Jankee/Gaunt (UCT) Feizifar/Abdulhadi (PNDC)	Second draft of report addressing reviews from B. Feizifar and I. Abdulhadi. Results from additional PHIL tests conducted between 15 – 17 August 2023 at DPSL were added. New results after re-synchronising the measurement data at PNDC and converting phase voltage measurements to line voltage measurements, were added.
06/11/2023	V3.0	Jankee/Gaunt (UCT) Feizifar/Abdulhadi (PNDC) Feng/Munro/Burt (DPSL)	Third draft of report addressing reviews from Feng/Munro/Burt.

Table of Contents

Executive Summary	11
1 Lab-Access User Project Information	14
1.1 Overview	14
1.2 Research Motivation, Objectives, and Scope	14
1.3 Structure of the Document	15
2 State-of-the-Art/State-of-Technology	16
3 Executed Tests and Experiments	18
3.1 Test Plan, Standards, Procedures, and Methodology	18
3.2 Test Set-up(s)	22
3.3 Data Management and Processing	31
3.4 Description of measurement systems at PNDC	31
4 Results and Conclusions	33
4.1 Discussion of Results	33
4.2 Conclusions	70
5 Open Issues and Suggestions for Improvements	72
References	73
Appendix A. Post-processing the PNDC measurements	75
A.1. Post-processing measurement data from Fluke meter	75
A.2. Post-processing measurement data from Beckhoff Data Acquisition System	76
Appendix B. Time-synchronisation of Fluke and Beckhoff Data Acquisition Systems	78
B.1. Test C1 - Synchronise Fluke D1 and Beckhoff D1	78
B.2. Test C1 - Synchronise Fluke F2, F1 and Beckhoff Data Acquisition Systems	80
B.3. Test C2 - Synchronise Fluke D1 and Beckhoff Data Acquisition Systems	84
B.4. Test C2 - Synchronise Fluke F2, F1 and Beckhoff Data Acquisition Systems	87
B.1. Investigation of Beckhoff timer drift	91
Appendix C. MATLAB script for post-processing and time synchronisation	93

List of Figures

Figure 1: Radial Feeder.....	12
Figure 2: Simple diagram of test system for DPSL and PNDC tests	18
Figure 3: Amended diagram of test system for DPSL tests.	19
Figure 4: Test A1.1 circuit diagram with source impedance parameters $R_{gen} = X_{gen} = 0.2645 \Omega$, transmission line parameters $R_{12} = X_{12} = 0.2116 \Omega$, $R_{23} = X_{23} = 0.3174 \Omega$, $R_n = X_n = 0.5290 \Omega$, and load parameters $R_a = R_b = R_c = 7.9350 \Omega$. The source voltage was initialised to 254.0430 V with phase A voltage angle = 5.1944°	23
Figure 5: Test A1.2 circuit diagram with same parameters as Test A1.1 except for load parameters $R_a = R_b = R_c = 5.7330 \Omega$ and $X_a = X_b = X_c = 3.5530 \Omega$	23
Figure 6: Test A1.1 circuit modelled in RSCAD. The software blocks used to interface the real-time simulated model and the 10 kW converter through the power amplifier is shown by current sources on the right of the diagram.	23
Figure 7: Test A1.2 circuit modelled in RSCAD. The software blocks used to interface the real-time simulated model and the 10 kW converter through the power amplifier is shown by current sources on the right of the diagram.	24
Figure 8: Test 1 circuit diagram with source impedance parameters $R_{gen} = X_{gen} = 0.2645 \Omega$, transmission line parameters $R_{12} = X_{12} = 0.2116 \Omega$, $R_{23} = X_{23} = 0.3174 \Omega$, $R_n = X_n = 0.5290 \Omega$, and load parameters $R_a = R_b = R_c = 7.9350 \Omega$. The source voltage was initialised to 254.0430 V with phase A voltage angle = 5.1944°	24
Figure 9: Test 2 circuit diagram with source impedance parameters $R_{gen} = X_{gen} = 0.2645 \Omega$, transmission line parameters $R_{12} = X_{12} = 0.2116 \Omega$, $R_{23} = X_{23} = 0.3174 \Omega$, $R_n = X_n = 0.5290 \Omega$, and load parameters $R_a = R_b = R_c = 5.7330 \Omega$ and $X_a = X_b = X_c = 3.5530 \Omega$. The source voltage was initialised to 254.0430 V with phase A voltage angle = 5.1944° ...	25
Figure 10: Hardware-In-the-Loop test bed	26
Figure 11: Photo of control room with multiple screens to monitor parameters and measured quantities in the 10 kW converter controller, RSCAD simulation model, the dc-power source and 90 kVA power amplifier. The 10 kW converter and 90 kVA power amplifier can also be observed in the experimental testing room.....	26
Figure 12: Connection diagram of test system at PNDC.	28
Figure 13: Photograph of 315 kVA 11/0.433 kV GMU-A step down transformer, LV cables. and load bank LB2	29
Figure 14: Photographs of 80 kW converter being connected to test bay D1 and regenerative controllable load	29
Figure 15: Test A1.1 results showing PoC V and I before compensation.....	33
Figure 16: Test A1.1 results showing PoC V and I during compensation.....	35
Figure 17: Test A1.1 results showing PoC V and injected compensating I during compensation	36
Figure 18: Test A1.2 results showing PoC V and I before compensation.....	37
Figure 19: Test A1.2 results showing PoC V and I during compensation	39
Figure 20: Test A1.2 results showing PoC V and injected compensating I during compensation.....	40
Figure 21: Test 1 Simulink results showing PoC V and I before compensation.	41
Figure 22: Test 1 RSCAD results showing PoC V and I before compensation.	41
Figure 23: Test 1 Simulink results showing PoC V and I during compensation.....	43
Figure 24: Test 1 RSCAD results showing PoC V and I during compensation.....	43
Figure 25: Test 2 Simulink results showing PoC V and I before compensation	45
Figure 26: Test 2 RSCAD results showing PoC V and I before compensation	45

Figure 27: Test 2 Simulink results showing PoC V and I during compensation.....	47
Figure 28: Test 2 RSCAD results showing PoC V and I during compensation.....	47
Figure 29: Test 3 Simulink results showing PoC V and I before compensation	49
Figure 30: Test 3 RSCAD results showing PoC V and I before compensation	49
Figure 31: Test 3 Simulink results showing PoC V and I during compensation.....	51
Figure 32: Test 3 RSCAD results showing PoC V and I during compensation.....	51
Figure 33: Test 4 Simulink results showing PoC V and I before compensation	52
Figure 34: Test 4 RSCAD results showing PoC V and I before compensation	53
Figure 35: Test 4 Simulink results showing PoC V and I during compensation.....	54
Figure 36: Test 4 RSCAD results showing PoC V and I during compensation.....	55
Figure 37: Test 5 Simulink results showing PoC V and I before compensation	56
Figure 38: Test 5 RSCAD results showing PoC V and I before compensation	57
Figure 39: Test 5 Simulink results showing PoC V and I during compensation.....	58
Figure 40: Test 5 RSCAD results showing PoC V and I during compensation.....	58
Figure 41: Test C1 Measured compensator output (solid lines) currents and controller's current references (dotted lines) generated from the PLL locked to phasor V_{BA}	63
Figure 42: Test C1 Measured compensator output (solid lines) currents and controller's current references (dot-ted lines) generated from the PLL locked to phasor V_{AN}	64
Figure 43: Sample .txt file produced using the export function from the Fluke meters. The data processing revealed irregular instances where a single timestamp appears multiple times, and each timestamp is associated with multiple values of the measured quantity.....	75
Figure 44: Comparison of measured Fluke data and up sampled data after post-processing using developed MATLAB script.	76
Figure 45: Comparison of original data with outliers and post-processed data after removing outliers	77
Figure 46: Test C1 - Unsynchronised voltage V_{AB} measured by Fluke and Beckhoff (bottom left waveform is in Fluke D1 seconds $s(F_{D1})$ and bottom right waveform is in Beckhoff D1 seconds $s(B_{D1})$)	78
Figure 47: Test C1 - Fluke voltages and currents plotted to find end of compensation time.	79
Figure 48: Test C1 - Synchronisation of Beckhoff and Fluke (top plot shows voltages and currents after being synchronised using the voltage spikes as reference, bottom left plot shows a zoomed-in image of the green-highlighted area from the top plot; it identifies the first zero-crossing the Fluke and Beckhoff voltages, before the end of compensation time, the bottom right plot shows a zoomed-in image of the bottom left; it identifies the time shift between the zero crossings. Time in $s(F_{D1})$	79
Figure 49: Test C1 - Synchronised Beckhoff and Fluke voltages and currents after zero-crossing matching. Time in $s(F_{D1})$	80
Figure 50: Test C1 - Identify the zero crossing in currents measured by Beckhoff D1, Fluke F1 and Fluke F2 around the end of compensation.	81
Figure 51: Test C1 - Synchronised Beckhoff D1, Fluke F1 and Fluke F2 measurements around the end of compensation.....	81
Figure 52: Test C1 - Identifying time interval t_1 before compensation.....	82
Figure 53: Test C1 - Identifying time interval t_2 during compensation.....	83
Figure 54: Test C1 - Identifying time intervals t_3 and t_4 - before and after compensation respectively	83
Figure 55: Test C2 - Unsynchronised voltage V_{AB} measured by Fluke and Beckhoff (bottom left waveform is in Fluke D1 seconds $s(F_{D1})$ and bottom right waveform is in Beckhoff D1 seconds $s(B_{D1})$)	85
Figure 56: Test C2 - Unsynchronised voltage V_{AB} measured by Fluke and Beckhoff (bottom left waveform is in Fluke D1 seconds $s(F_{D1})$ and bottom right waveform is in Beckhoff D1 seconds	

s(B_{D1}) 85

Figure 57: Test C2 - Synchronisation of Beckhoff and Fluke (top plot shows voltages and currents after being synchronised using the voltage spikes as reference, bottom left plot shows a zoomed-in image of the green-highlighted area from the top plot; it identifies the first zero-crossing the Fluke and Beckhoff voltages, before the end of compensation time identified from Fluke D1 currents, the bottom right plot shows a zoomed-in image of the bottom left plot; it identifies the time shift between the zero crossings. Time in s(F_{D1}) 86

Figure 58: Test C2 - Synchronised Beckhoff and Fluke voltages and currents after zero-crossing matching. Time in s(F_{D1}). 87

Figure 59: Test C2 - Identify the zero crossing in currents measured by Beckhoff D1, Fluke F1 and Fluke F2 around the end of compensation. 88

Figure 60: Test C2 - Synchronised Beckhoff D1 and Fluke D1 measurements around the end of compensation instant 88

Figure 61: Test C2 - Identifying time interval t1 before compensation..... 89

Figure 62: Test C2 - Identifying time interval t2 during compensation. 89

Figure 63: Test C2 - Identifying time intervals t3 and t4, before and after compensation respectively. 90

Figure 64: Fluke D1 and Beckhoff D1 voltages during different periods after synchronisation shows that there is a drift in the Beckhoff Data Acquisition System over time. 92

List of Tables

Table 1: Test plan on arrival at University of Strathclyde.....	18
Table 2: Amended test plan for 10 kW inverter in DPSL.....	20
Table 3: Amended test plan for 80 kW inverter in PNDC.	20
Table 4: Final test plan for 10 kW inverter in DPSL.	21
Table 5: Final test plan for 80 kW inverter in PNDC.	21
Table 6: Additional test plan for 10 kW inverter in DPSL.	21
Table 7: Position of meters for tests at PNDC.....	27
Table 8: Specifications of the 80 kW inverter used in PNDC.....	28
Table 9: Measurement record on a spreadsheet.....	32
Table 10: Test A1.1 Inputs to GPT spreadsheet before compensation.....	34
Table 11: Test A1.1 Calculated powers, losses, minimum loss, power factor and apparent power before compensation.....	34
Table 12: Test A1.1 Calculated optimal compensating currents before compensation.....	35
Table 13: Test A1.1 Inputs to GPT Spreadsheet during compensation.....	35
Table 14: Test A1.1 Calculated powers, losses, minimum loss, power factor and apparent power during compensation.....	36
Table 15: Test A1.1 Fundamental frequency reference and injected compensating currents.....	37
Table 16: Test A1.2 Inputs to GPT Spreadsheet before compensation.....	38
Table 17: Test A1.2 Calculated powers, losses, minimum loss, power factor and apparent power before compensation.....	38
Table 18: Test A1.2 Calculated optimal compensating currents before compensation.....	38
Table 19: Test A1.2 Inputs to GPT Spreadsheet during compensation.....	39
Table 20: Test A1.2 Calculated powers, losses, minimum loss, power factor and apparent power during compensation.....	40
Table 21: Test A1.2 Fundamental frequency reference and injected compensating currents.....	40
Table 22: Test 1 Inputs to GPT Spreadsheet before compensation.....	42
Table 23: Test 1 Calculated powers, losses, minimum loss, power factor and apparent power before compensation.....	42
Table 24: Test 1 Calculated optimal compensating currents before compensation.....	42
Table 25: Test 1 Inputs to GPT Spreadsheet during compensation.....	44
Table 26: Test 1 Calculated powers, losses, minimum loss, power factor and apparent power during compensation.....	44
Table 27: Test 1 Fundamental frequency reference and injected compensating currents.....	45
Table 28: Test 2 Inputs to GPT Spreadsheet before compensation.....	46
Table 29: Test 2 Calculated powers, losses, minimum loss, power factor and apparent power before compensation.....	46
Table 30: Test 2 Calculated optimal compensating currents before compensation.....	47
Table 31: Test 2 Inputs to GPT Spreadsheet during compensation.....	48
Table 32: Test 2 Calculate powers, losses, minimum loss, power factor and apparent power during compensation.....	48
Table 33: Test 2 Reference and injected compensating currents.....	48
Table 34: Test 3 Inputs to GPT Spreadsheet before compensation.....	49
Table 35: Test 3 Calculated powers, losses, minimum loss, power factor and apparent power before	

compensation.....	50
Table 36: Test 3 Calculated optimal compensating currents before compensation	50
Table 37: Test 3 Inputs to GPT Spreadsheet during compensation	51
Table 38: Test 3 Calculate powers, losses, minimum loss, power factor and apparent power during compensation.....	52
Table 39: Test 3 Reference and injected compensating currents.....	52
Table 40: Test 4 Inputs to GPT Spreadsheet before compensation	53
Table 41: Test 4 Calculated powers, losses, minimum loss, power factor and apparent power before compensation.....	54
Table 42: Test 4 Calculated optimal compensating currents before compensation	54
Table 43: Test 4 Inputs to GPT Spreadsheet during compensation	55
Table 44: Test 4 Calculated powers, losses, minimum loss, power factor and apparent power during compensation.....	56
Table 45: Test 4 Reference and injected compensating currents.....	56
Table 46: Test 5 Inputs to GPT Spreadsheet before compensation	57
Table 47: Test 5 Calculated powers, losses, minimum loss, power factor and apparent power before compensation.....	57
Table 48: Test 5 Calculated optimal compensating currents before compensation	58
Table 49: Test 5 Inputs to GPT Spreadsheet during compensation	59
Table 50: Test 5 Calculated powers, losses, minimum loss, power factor and apparent power during compensation.....	59
Table 51: Test 5 Reference and injected compensating currents.....	60
Table 52: Test C1 h1 CRMS values of V and I at each bus before compensation t1 (B: Beckhoff; F: Fluke).	60
Table 53: Test C1 h1 CRMS values of V and I at each bus before compensation t2 (B: Beckhoff; F: Fluke).	61
Table 54: Test C1 h1 CRMS values of V and I at each bus before compensation t3 (B: Beckhoff; F: Fluke).	61
Table 55: Test C1 h1 CRMS values of V and I at each bus before compensation t4 (B: Beckhoff; F: Fluke).	61
Table 56: Test C1 Fundamental frequency power at each bus at different time intervals.....	62
Table 57: Test C1 Fundamental frequency power loss in each branch at different time intervals	62
Table 58: Test C1 Fundamental frequency power measurements and derived resistances R1-2 and R2-3 in Ohms per 100 m in each branch at different time intervals	63
Table 59: Test C2 h1 CRMS values of V and I at each bus before compensation t1 (B: Beckhoff; F: Fluke).	65
Table 60: Test C2 h1 CRMS values of V and I at each bus before compensation t2 (B: Beckhoff; F: Fluke).	65
Table 61: Test C2 h1 CRMS values of V and I at each bus before compensation t3 (B: Beckhoff; F: Fluke).	65
Table 62: Test C2 h1 CRMS values of V and I at each bus before compensation t4 (B: Beckhoff; F: Fluke).	65
Table 63: Test C2 Fundamental frequency power at each bus at different time intervals.....	66
Table 64: Test C2 Fundamental frequency power loss in each branch at different time intervals	66
Table 65: Test C2 Fundamental frequency power measurements and derived resistances R ₁₋₂ and R ₂₋₃ in Ohms per 100 m in each branch at different time intervals	66
Table 66: Test C2 – Frequency of each current cycles and adjacent cycles in A-phase at Bus 1 during each time interval. Note measurements at bus 1 were made using Fluke meter F2.	67

Table 67: Test C2 – Frequency of each current cycles and adjacent cycles in A-phase at Bus 2 during each time interval. Note measurements at bus 2 were made using Fluke meter F1. 67

Table 68: **h1** CRMS values of V and I at each bus **before compensation t1** (B – Beckhoff and F – Fluke). 68

Table 69: **h1** CRMS values of V and I at each bus **during compensation t2** (B – Beckhoff and F – Fluke). 68

Table 70: **h1** CRMS values of V and I at each bus **during compensation t3** (B – Beckhoff and F – Fluke). 68

Table 71: **h1** CRMS values of V and I at each bus **after compensation t4** (B – Beckhoff and F – Fluke). 69

Table 72: Fundamental frequency power at each bus and different time intervals..... 69

Table 73: Fundamental frequency power loss in each branch at different time intervals 69

Table 74: Test C1 Fundamental frequency power measurements and derived resistances R1-2 and R2-3 in Ohms per 100 m in each branch at different time intervals 69

Table 75: Description of chosen time intervals for analysing the results (Applies both to tests C1 and C2) 82

Table 76: Test C1 – Resulting time shifts or correction factors to apply to Fluke measurements such that they align to the Beckhoff measurements during different time intervals used for analysis 84

Table 77: Test C1 - Time intervals for analysis in $s(B_{D1})$, $s(F_{F1})$, $s(F_{F2})$ and frequency used for FFT. 84

Table 78: Test C2 - Resulting time shifts or correction factors to apply to Fluke measurements such that they align to the Beckhoff measurements during different time intervals used for analysis 90

Table 79: Test C2 - Time intervals for analysis in $s(B_{D1})$, $s(F_{F1})$, $s(F_{F2})$ and frequency used for FFT. 91

Table 80: Results from the analysis of the Beckhoff timer drift showing a small ratio of the cycle-periods measured by Beckhoff D1 and Fluke D1. 92

List of Abbreviations

CO	Project Coordinator
CRMS	Complex Root Mean Square
CHIL	Controller-Hardware-in-the-Loop
DFT	Discrete Fourier Transform
DG	Distributed Generation
EC	European Commission
FFT	Fast Fourier Transform
GPT	General Power Theory
HV	High Voltage
LA	Lab Access
LV	Low Voltage
MIU	Mock Impedance Unit
MV	Medium Voltage
PHIL	Power-Hardware-in-the-Loop
PLL	Phase Locked Loop
PoC	Point of Connection
PWM	Pulse Width Modulation
RMS	Root Mean Square
RTDS	Real Time Digital Simulator
TEI	Thévenin Equivalent Impedance
THD	Total Harmonic Distortion
UCT	University of Cape Town
UG	User Group
UP	User Project

Executive Summary

This report summarises the objective, execution, results, and conclusions of testing carried out under the ERIGRID 2.0 project Advanced GPT Inverter Physical Demonstration (AGIPDem) at the University of Strathclyde from 12 April to 5 May 2023 by two Users from the University of Cape Town (UCT).

The objective of the testing was to demonstrate the effects on power systems of an inverter operating under General Power Theory (GPT) control. The derivation of the novel power theory, (which does not accommodate or use the concept of reactive power), some simulation studies, and description of the application for inverter control have been published already. It was expected that the GPT-controlled inverter would reduce system power loss and change voltages at the terminals of a simple 3-node radial feeder, without reducing the power delivered.

Executed tests

The plan was to operate a modified commercial 80 kW 3-phase 3-wire inverter manufactured by ArioGenix, retro-fitted and supplied by UCT, and measure the system response to a variety of already simulated system loading conditions. Power Hardware-in-the-Loop (PHIL) tests were to be made in the Dynamic Power Systems Laboratory (DPSL), and physical tests in the Power Networks Demonstration Centre (PNDC). Delayed delivery of the inverter to be tested required a change in plan and a one-week extension of the arranged two-week testing period.

When the extent of delay in the inverter delivery from South Africa became evident, the Host agreed to a suggestion that an existing 10 kW 3-phase 4-wire inverter in the DPSL be retro-fitted with GPT-control.

This was carried out by re-programming the controller of the host inverter. A few days were spent reconciling the simulator's models of power system components and programming in RSCAD with the MATLAB software and simulations. The testing was limited by the stable operation of the test bed, the limits of the DC supply, and the inverter's phase locked loop (PLL) that was capable of processing only sinusoidal waveforms. In the time available, measurements were obtained for two of the planned 12 tests. (After discussion with the Director of the Institute for Energy and Environment, one of the original tests was repeated and four more PHIL tests were carried out using the same 10 kW inverter from 15 to 17 August 2023.)

By the time the 80 kW inverter was received, the high-voltage DC power supply hired by the DPSL was no longer available, so the inverter was sent directly to the PNDC laboratory.

At the PNDC, a 3-node radial feeder was supplied from the local distribution network operator through an isolation transformer and a 315 kVA ground-mounted substation, as illustrated in Figure 1. Three data acquisition instruments were installed in the feeder at Bus 1, Bus 2, and Bus 3. A fourth instrument was installed in the connection from the inverter at Bus 3. Adjustable load banks were connected to Bus 3, and a grid emulator at Bus 2.

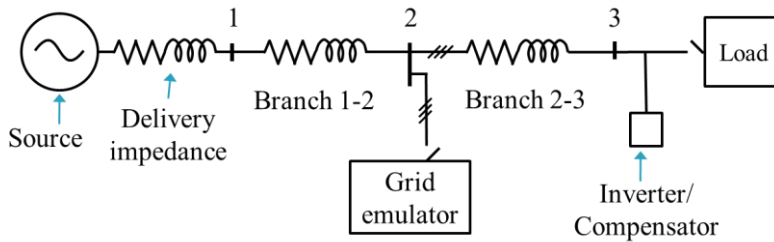


Figure 1: Radial Feeder

Various unexpected delays in setting up the networks and measurement systems had the effect of limiting the experiment to only two of the seven planned feeder loading cases.

Post-processing the data collected at PNDC was necessary to synchronise the measurements and correct time-clock drift in one of the data collection instruments. The process is described in detail in Appendices A, B, and C.

Results

The results obtained from testing the Host's 10 kW converter in DPSL showed that the GPT compensates for the avoidable loss when supplying a balanced resistive and inductive load without the need to use reactive power as a concept in the inverter control.

Despite meticulous synchronisation of the data collected at PNDC, a reality check of the currents and power measured during four 2-cycle periods at each bus gave inconsistent estimates of the resistance of each of the two branches 1-2 and 2-3 before, during, and after inverter current was injected at Bus 3. Such performance is physically unexplainable.

The post-processing also revealed an error in setting the reference voltage in the inverter controller (set to a phase-neutral voltage reference instead of a line-line reference). This had the result that the currents injected by the inverter were not those for optimal loss reduction but other currents instead. This was inconvenient but not disastrous as the physical measurements of system performance can be inputs into a software simulation, and eventually the optimum current injection run in the same system would show the performance expected from the optimal current injection. However, the radial feeder configuration and metering at all busbars allow a reality check of the voltage, current and power measurements given an expectation that the resistances of the cables 1-2 and 2-3 remained constant. Varying and inconsistent values of branch resistances based on the measurements make interpretation of the results difficult.

After discussions between the UG and PNDC staff, it was evident that the data acquisition system (Beckhoff DAQ) measured phase voltages with respect to a virtual neutral instead of line voltage measurements as required for the tests. This meant that the input quantities of voltage used to calculate the reference currents for the converter were not correct and therefore, compensation using those current values would not have given the expected results even if the PLL was configured correctly.

Irrespective of whether the apparent variable results of the power, current and cable resistance reality check were the result of cabling, metering or inverter problems, no coherent conclusions about the inverter control and power system performance can be drawn from the results of the tests at the PNDC.

Conclusions

PHIL simulation testing and results depend significantly on the available models of power system components. Six sets of useful results were obtained at the DPSL, which together demonstrate the validity of the GPT approach to measurement, control, and system performance.

There is a non-negligible measure of uncertainty that the Fluke and Beckhoff Data Acquisition Systems were not recording consistent voltage and current data suitable for the level of processing needed to implement the experiment. Further, other possible sources of experimental uncertainty have been identified. Although no directly useful results from the real-lab tests were obtained to confirm the effects of GPT control on power system performance, valuable experience was gained that will lead to successful tests in the future.

1 Lab-Access User Project Information

1.1 Overview

The testing under the ERIGrid 2.0 project Advanced GPT Inverter Physical Demonstration (AGIPDem) took place during the period 12 April to 5 May 2023 at Strathclyde University using the Dynamic Power Systems Laboratory (DPSL) and Power Networks Demonstration Centre (PNDC). The UG members were Trevor Gaunt and Pitambar Jankee.

The scope of the application included a four-week period of testing, but the budget granted required that the programme be reduced to two weeks. Delayed delivery of the inverter to be tested and various unforeseen problems during testing required a change in the test scope and an additional one-week extension. The testing protocols were revised as testing proceeded, and the participation during the second week of a third UG member, Michel Malengret was canceled. Approximately equal time was spent in each of the DPSL and the PNDC.

The report identifies the tests, problems, revisions, and analysis that produced useful conclusions from the measurements.

1.2 Research Motivation, Objectives, and Scope

In most countries, existing central power stations are likely – at least in part – to be replaced by smaller renewable energy sources of generation capacity typically 10 kW to 300 MW and distributed widely throughout the network, including at low (400 V), medium (11 kV) and high voltage. Decentralised battery storage installations are also likely. Most (or all) of the renewable energy and battery sources require power electronic inverters to connect each source to the power system.

Compounding the above changes, electricity users are distributed over wide geographical areas and exhibit variable daily demand/consumption profiles, unbalance, and distortion of the standard sinusoidal ac supply, especially towards the ‘grid-edge’. The load unbalance and waveform distortion result in significant avoidable losses in the distribution systems (sometimes as high as 10%) with few options to reduce these losses. Optimally reducing distribution losses could reduce carbon emissions by making more generated electricity available for consumption, reduce utility costs, and improve the economic contribution of electricity supply.

All large/mini/micro/smart grids with renewable energy and new energy flow patterns drive the need for new technologies to optimise the energy transmission and reduce losses.

UCT has been researching power flow in networks. A novel General Power Theory (GPT) that can achieve the optimisation through dynamically balancing and re-shaping currents in the different wires of an electricity distribution network has been developed and published (Malengret and Gaunt), and patented (UCT). The GPT was developed on a physics-consistent concept (or measurement) model and derived rigorously in linear algebra. Its effects have been successfully demonstrated in computer simulation and with a small-scale technology concept implementation of a compensator. The GPT challenges the 100-year-old power theory that underlies most conventional approaches to power systems.

To win acceptance of the novel approach and applications, the validity of the GPT needs to be

tested in a physical power system. The approach proposed was to convert to GPT-control a commercial 3-phase converter and, after CHIL and PHIL simulations, operate it as a compensator and inverter under steady-state conditions in an independent laboratory's mini/micro grid.

The objective of the proposed laboratory experiments was to demonstrate in physical power circuits the practical validity of the GPT.

- 1) The demonstrations were expected to show that the delivery loss attributable to a load or source at its Point of Connection (PoC) can be measured by the GPT approach using only measurements at the PoC and for a variety of practical conditions of unbalance and waveform distortion.
- 2) The tests should demonstrate that it is possible to reduce, even eliminate, avoidable loss using a GPT-controlled inverter between PV-, wind- and battery-sources and the delivery network.
- 3) The tests should demonstrate that the practical application of the concepts of reactive power and its derivatives cannot define the physical operation of the power system as effectively as the GPT, especially under conditions of unbalance between the wires of the system and distortion of the waveforms, which commonly characterise the conditions at the grid-edges and in isolated small grids.

Once the physics-consistent validity of the GPT has been demonstrated, there will be significant implications for the definitions of power parameters and measurement in international and national standards. Large gaps in teaching and research will need to be filled, and new approaches to metering, control, power system analysis, and electricity policy and regulation will need to be developed.

1.3 Structure of the Document

This document is organised as follows: Section 2 briefly outlines the state-of-the-art/state-of-technology that provides the basis of the realised Lab Access (LA) User Project (UP). Section 3 briefly outlines the performed experiments. Section 4 summarises the results and conclusions. Potential open issues and suggestions for improvements are discussed in Section 5. Finally, additional information is provided in the Appendix A. Post-processing the PNDC measurements; Appendix B. Time-synchronisation of Fluke and Beckhoff Data Acquisition Systems; and Appendix C. MATLAB script for post-processing and time synchronisation.

2 State-of-the-Art/State-of-Technology

Many concept models, theories, and definitions of electric power have been proposed during the past 130 years. Most models are based on mathematics but lack a solid physics foundation and make assumptions that are violated in practical systems.

Meanwhile, technology trends are changing modern power systems from those of the 20th century. The increasing use of intermittent renewable energy that requires backup from dispatchable energy sources is linked to their distribution closer to the edges of power systems, where distortion and phase unbalance are significant. Power electronics technology can change the characteristics of loads, storage, and many sources, and digital techniques have replaced most analogue measurement and control.

Most electrical standards define power components for an apparatus that is for a device or an assembly of circuit elements or devices comprising a load. Only a few power theories define the components of power in the context of a power system.

The terms of apparent power, wattless power, power factor and the impedance triangle were introduced in the 1890s. In 1910, Kennelly extended the impedance triangle to power and energy. By 1920 it was “desirable” to treat phase displacement, unbalance, and waveform distortion as separate effects, and this approach has been widely adopted to the present.

The first version of the GPT was published in 2008 [1]. It was followed by three papers on instantaneous power [2], average power [3] and power measurement [4]. These early papers included reviews of the older theories of Fryze, Depenbrock and Buchholtz, and more modern theories of Akaji, Willems, Ferrero, Nabae, Rossetto, Peng, Dai, Salmerón, Filipowski, Czarnecki, Jeon, Morsi, Emanuel, Mayordona, Mishra, Montero, Ustariz, Atefi, and their co-authors. Some of these, and others, have been identified by Simoes et al [5] in a more recent review of time domain theories.

The GPT was extended to the frequency domain to accommodate frequency-dependent impedances. It is described in a granted patent [6] and a detailed description of the derivation and proof of the theory [7]. The theory development paper included reviewing recent developments of the p-q, conservative power and current physical components theories, and other approaches, by Czarnecki, Burgos-Mellado, Schäffer, Montoya, Moriano, Monteiro, Dey, Mikulović, Jeon, Bhattarai, Lev-Ari, and their co-authors.

Important outcomes of the physics-consistent model and algebraic rigour of the GPT are that no parameter of reactive power can be identified, and the non-active component of current measured at a point of connection (incurring delivery loss but not contributing to power delivery) is not orthogonal to the active component of current. As a result, analysis incorporating Q or Q-loss or p-q theory can only be approximations of the physical behaviour of systems.

There are practical implications of the inadequacies of conventional power theory in the presence of unbalance and waveform distortion. The multiple inconsistent definitions of power components (apparent and reactive power, and power factor) lead to different measurement results [8] and disputes with customers [9]. Smart meters can even display export power in the absence of behind-the-meter generation [10]. Power theory also provides the basis for control and compensation and the GPT addresses control in the steady state.

In this project, the control of the current injection is more significant than the design and operation of the converter itself. The separate control of the individual phases was

demonstrated in our concept test of a compensator [11]. The technologies of power electronic converters (compensators and inverters) are covered extensively in the technical literature.

The controller calculates the reference compensating currents and produces PWM signals to control the power electronic switches. Reference currents calculated using conventional power theories perform well under sinusoidal balanced conditions but become inaccurate under non-sinusoidal and unbalanced conditions [12], [13]. Controllers based on reactive power concepts lack physical meaning and those employing $0\alpha\beta$ or $dq0$ transforms increase controller complexity. The non-zero neutral current after compensation in unbalanced systems requires a dc-link capacitor voltage to be controlled by one of various methods [14].

Some of the implications of the GPT have been demonstrated by simulation of the effects of distortion and unbalance on power systems [15], [16], [17], [18].

Practical demonstration of a GPT-controlled inverter and its effect on a real power system in an independent laboratory was made possible by this ERIGrid project.

3 Executed Tests and Experiments

3.1 Test Plan, Standards, Procedures, and Methodology

3.1.1 Test Plan on Arrival

The nature of the proposed testing was not to test a converter, but to test its effect on the losses and voltages of a distribution system when operated as a load compensator or as an inverter injecting power into the system. The system is illustrated in the diagram of Figure 2.

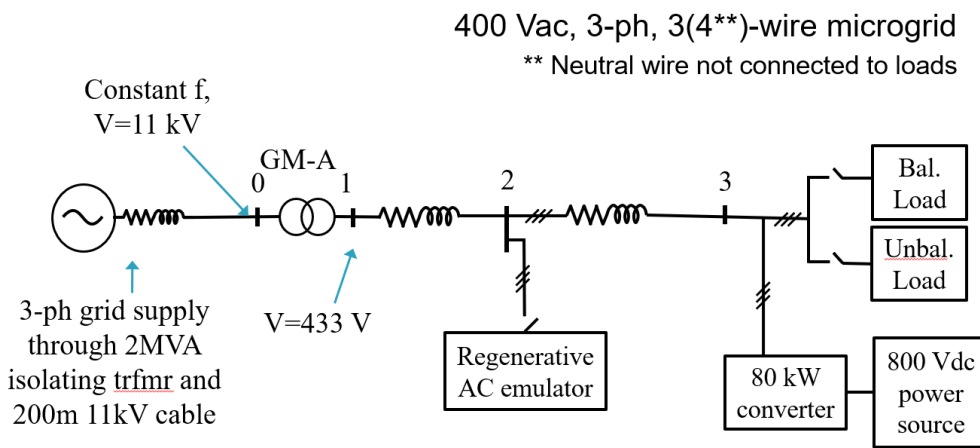


Figure 2: Simple diagram of test system for DPSL and PNDC tests

The proposed plan was to use an 80 kW 400 V 3-phase 3-wire inverter commercially produced by ArioGenix in South Africa. It had been modified at the factory to use GPT-control or its original conventional control according to the setting of an electronic switch. Before despatch, factory tests had been carried out with an isolated grid emulator and with the converter connected to the national electricity network.

Four series of tests were planned, shown in Table 1. Series A and B were respectively for load compensation and power injection by the inverter as distributed generation (DG) at DPSL. Series C and D tests were similar for compensator and inverter operation at PNDC.

Table 1: Test plan on arrival at University of Strathclyde.

DPSL	PNDC	Constant power Load at Bus 3 (Load = + and Source= -)				Keysight at Bus 2 (Load = + and Source= -)			Compensation
		RX	Total balanced load	Total unbalanced load	Distorted load	Lump/cabled	Total balanced load	Total unbalanced load	
A1.1a		R	200 kW			Lump			NG
A1.1b	C1	R	200 kW			Cable			NG
A1.2		RX	200 kVA			Lump			NGC
A2.1		R		150 kW 1ph		Lump			NG
A2.2		RX		150 kVA 1ph		Lump			NG
A2.3	C2	RX	200 kVA	17/30 kVA		Cable			NG
A3	C5	RX	200 kVA		-h5,7 50 kVA	Lump			NG
A4	C6	RX	200 kVA	17/30 kVA	-h5,7 50 kVA	Lump			NG
A5	C4	R	200 kW			Cable		RX all diff 50kVA total	NGC
A6		RX	200 kVA			Cable		+h5,7 50 kVA	NGC
A7.1		RX	200 kVA			Cable		+h2,4,5,7	NGC
A7.2	C3	RX	200 kVA			Lump		-h2,4,5,7	NGC
B1		RX	0, 20, 28, 36, 60, 80			Lump	100 kVA		NG
B2		RX	0, 40, 80			Lump	100 kVA		NG
B3		RX	0, 40, 80			Lump	100 kVA		NG
B4	D1	RX	0, 20, 28, 36,			Lump	50 kVA		NGC
B5		RX	0, 20, 40, 60, 80			Lump	100 kVA	3% unbal	NGC

The test plan was delivered to the HI before arrival.

3.1.2 Amended Test Plan

On arrival at DPSL, it was discovered that the 80 kW inverter despatched from the factory in South Africa had been delayed and could not be used for the planned tests at DPSL. It was re-directed to PNDC, where it arrived on Tuesday 25 April.

The UG asked the Host Director whether it would be allowed to convert a 3-phase 4-wire 10 kW converter already in the DPSL. Permission was given and GPT-control was programmed onto the converter. This took 4 days. The conventional current control system of the 10 kW inverter is implemented in MATLAB Simulink and so is the GPT control system which was integrated to the 80 kW converter. After re-calculating the controller gains based on the specifications of the 10 kW converter including the LCL filter, a frequency-domain and time-domain analysis in MATLAB and Simulink respectively, the GPT-based current controller was integrated onto the 10 kW converter. No changes to the measurements were required since all required measurement inputs to the controller were already available and being used in the conventional control system.

The smaller converter did not require the 800 V dc power supply arranged by the DPSL. When the GPT-controlled converter was tested with the grid emulator, the controller proved to be stable and tracked the reference currents with negligible steady-state errors. Although the GPT-current controller was stable with the grid emulator, there were difficulties in interfacing the converter with the RTDS simulator. Random trips occurred on start-up of the dc-power source and converter. When the trip condition did not assert, we managed to test the GPT-current controller starting from the fundamental frequency controller and successively adding harmonic current controllers. This took almost 3 days due to the need to debug and random but frequent tripping of the converter.

The amended test setup was changed to that of *Figure 3*. The test plan for DPSL was reduced in scope to that shown in Table 2.

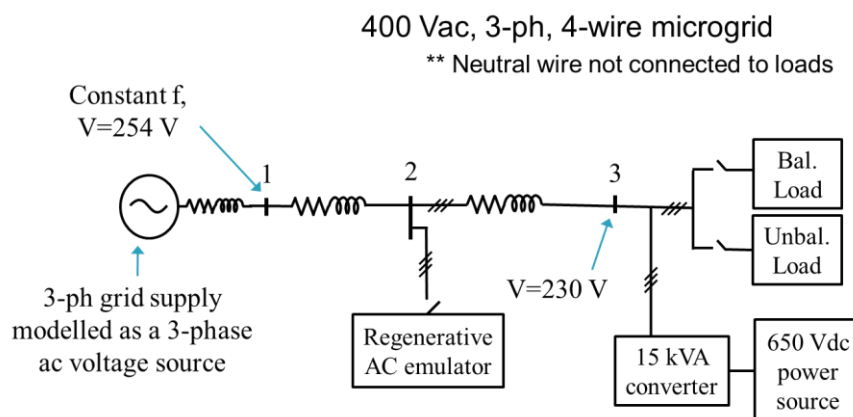


Figure 3: Amended diagram of test system for DPSL tests.

Table 2: Amended test plan for 10 kW inverter in DPSL.

DPSL	Constant power Load at Bus 3 (Load = + and Source= -)				Keysight at Bus 2 (Load = + and Source= -)			Compensation	
	RX	Total balanced load	Total unbalanced load	Distorted load	Lump/cabled	Total balanced load	Total unbalanced load	Distortion	None/GPT/Conv
A1.1a	R	20 kW			Lump				NG
A1.1b	R	20 kW			Cable				NG
A1.2	RX	20 kVA			Lump				NGC
A2.1	R		5 kW 1ph		Lump				NG
A2.2	RX		5 kVA 1ph		Lump				NG
A2.3	RX	15 kVA	5 kVA		Cable				NG
A3	RX	25 kVA		-h5,7 50 kVA	Lump				NG
A4	RX	20 kVA	5 kVA	-h5,7 50 kVA	Lump				NG
A5	R	14.4 kW			Cable		1.8 kVA @ 0.85 IF Phase A 1.8 kVA @ 0.90 IF Phase B		NGC
A6	RX	25 kVA			Cable			+h5,7 5 kVA	NGC
A7.1	RX	20 kVA			Cable			+h2,4,5,7	NGC
A7.2	RX	20 kVA			Lump			-h2,4,5,7	NGC
B1	RX	0, 10, 15			Lump	20 kVA			NG
B2	RX	0, 10, 15			Lump	21 kVA	As A5		NG
B3	RX	0, 10, 15			Lump	22 kVA		30%-h5 20%-h7	NG
B4	RX	0, 10, 15, 23			Lump		20 kVA	50%-h1 30%-h5 20%-h7	NGC
B5	RX	0, 10, 15			Lump	20 kVA	3% unbal	5% THD	NGC

When the 80 kW converter arrived at PNDC, it took one day to set up the converter and configure the physical power network. Recognising that the available time was constrained, the test plan was shortened to that in Table 3.

Table 3: Amended test plan for 80 kW inverter in PNDC.

PNDC	Constant power Load at Bus 3 (Load = + and Source= -)				Keysight at Bus 2 (Load = + and Source= -)			Compensation	
	RX	Total balanced load	Total unbalanced load	Distorted load	Lump/cabled	Total balanced load	Total unbalanced load	Distorted load	None/GPT/Conv
C1	R	200 kW			Cable				NG
C2	RX	200 kVA	17 kVA		Cable				NG
C3	RX	200 kVA			Cable				NG
C4	R	200 kW			Cable		RX all diff 50kVA total		
C5	RX	200 kVA		-h5,7 50 kVA	Cable				NG
C6	RX	200 kVA		-h5,7 50 kVA	Cable				NG
D1	RX	0, 20, 28, 36			Cable	50 kVA		+/- h1, -h5, -h7	NGC

3.1.3 Final Test Plan

Although it was agreed to extend the laboratory time for one member of the UG for a third week, several unexpected problems that arose at both laboratories had the effect of limiting the scope of tests that could be carried out.

At DPSL, after having tested the GPT-based current controller connected to the RTDS, additional software and controller problems came up. We experienced modelling challenges in RSCAD to interface the high-frequency switching model of a rectifier (causing distortion of voltages and currents) and the low-frequency models of the power system components. Therefore, we attempted 3 alternative approaches which used controlled current sources to mimic the current drawn or injected by the rectifier. This took 3 days until we managed to inject or draw harmonic currents into the test network. When we started testing the effect of GPT control on system performance, we found that the phase-lock-loop (PLL) of the 10 kW inverter did not work with distorted and/or unbalanced voltage waveforms, with the effect that none of the tests with waveform distortion and unbalance (A2 – A7.2 and B2 – B5) were possible. Due to the RSCAD software limitations and modelling challenges, we designed a simple 2-bus test network for PHIL

tests at DPSL.

At PNDC, the experimental tests were delayed due to several non-considered factors when planning the experiments. The first was that a shortage of measuring instruments required the use of a laboratory-assembled uncalibrated instrument (Beckhoff Data Acquisition System) that was available and had to be connected into the circuits. A second problem arose from the limited harmonic power capacity of the Keysight load emulator so that the loads needed to be re-configured to maximise the distortion at the PoC that could be achieved. Last, it was recognised that the inverter operation was not giving the load reduction expected, and significant time was spent (after returning to Cape Town) in identifying that the problem was that an electronic switch to select PLL lock to a phase-neutral or phase-phase reference voltage was in the wrong 'position' and the converter currents were not being injected at the correct phase angle. However, even if the PLL inputs were correct, the results would still not be correct since the DAQ system used to collect measurements at the Point of Connection was also incorrectly set to measure phase voltages instead of line voltages. As a result of the delays caused, only two of the planned tests could be completed.

Table 4 and Table 5 show the final tests implemented at DPSL and PNDC respectively.

Table 4: Final test plan for 10 kW inverter in DPSL.

DPSL	Constant power Load at Bus 3 (Load = + and Source= -)					Keysight at Bus 2 (Load = + and Source= -)			Compensation
	RX	Total balanced load	Total unbalanced load	Distorted load	Lump/cabled	Total balanced load	Total unbalanced load	Distortion	None/GPT/Conv
A1.1b	R	20 kW			Cable				NG
A1.2	RX	20 kVA			Cable				NGC

Table 5: Final test plan for 80 kW inverter in PNDC.

PNDC	Constant power Load at Bus 3 (Load = + and Source= -)					Keysight at Bus 2 (Load = + and Source= -)			Compensation
	RX	Total balanced load	Total unbalanced load	Distorted load	Lump/cabled	Total balanced load	Total unbalanced load	Distorted load	None/GPT/Conv
C1	R	50 kW			Cable				NG
C2	RX	50 kVA	17 kVA		Cable				NG

3.1.4 Additional tests carried out at DPSL

Realising the possibility of doing further tests using the modified 10 kW inverter at DPSL, the UG engaged with the Host Director, to request remote testing A series of 5 PHIL tests were carried out remotely between 15 to 17 August 2023.

Table 6 shows the five additional tests carried out at DPSL.

Table 6: Additional test plan for 10 kW inverter in DPSL.

Test	RX	Total balanced load	Total unbalanced load	Tx line X/R ratio	Remarks
1	R	20 kW		1	Redo test A1.1b of April 2023
2	RX	20 kW		1	Test A1.2 of April 2023
3	R	25 kW		4	Test 1 but with different network parameters
4	RX	34 kW		1.5	Test 2 but with different network parameters (Source inductance was removed and load inductance set to 1 mH)
5	R		10 kW phA 9 kW phB 9.5 kW phC	1	Test with small unbalance

Remarks:

1. When PHIL test A1.1b was carried out in April 2023, the results were not captured within a steady-state time interval. Therefore, the PHIL test 1.1b was repeated, and new results were collected.
2. PHIL test A1.2 results were correct when the test was done in April 2023. The results were already available.
3. PHIL test 3 was carried out with a new set of network parameters; the load power was increased to 25 kW and the X/R ratio of the transmission line was changed to 4.
4. PHIL test 4 was supposed to use the same parameters as test 3 except for the load. However, we experienced instability issues when using too-high inductance in the test circuit. Hence, the X/R ratio of the line was reduced until a satisfactory stable response was observed. This was carried out by sequentially varying the X/R ratio and calculating the equivalent R and L on a spreadsheet. An inductive load of 1 mH with the same resistance as test 3 was chosen for test 4.
5. PHIL test 4 was carried out to show the effect of GPT-compensation for an unbalanced resistive load. Initially, we planned to generate at least 10 % voltage unbalance (as per NEMA definition). However, during the PHIL testing, we realised that the PHIL test bed was not designed to handle such levels of unbalance. We therefore revised the load parameters to generate a relatively small unbalance in the network.

3.2 Test Set-up(s)

3.2.1 PHIL Tests at DPSL

The base test network was designed as a three-phase four-wire system supplying a balanced 20 kW resistive load and initialised such that the phase voltage at the point of connection (PoC) was 230 V. This base test model was called test A1.1, for which the delivery system impedance was modelled with an X/R ratio of 1. The values of R and X were determined by imposing a constraint that there should be 10 % of power delivery loss (2 kW) when supplying a 20 kW load. The second test system, test A1.2, used the exact same circuit parameters and initialisation conditions but with a 20 kW resistive and inductive load having an impedance factor of 0.85. Power Hardware-in-the-Loop (PHIL) simulations of tests A1.1 and A1.2 were carried out by injecting compensating currents using the physical 10 kW converter available at the DPSL.

Figure 4 shows the base case test network which was developed using a 20 kW load with 10 % voltage drop from the source to the PoC and 10 % or 2 kW power delivery loss. Figure 5 shows the base case test network which was developed using a 20 kW resistive and inductive load with an impedance factor of 0.85. The transmission line impedance and generator impedance were left unchanged in test A1.2. The generator terminal voltage was also left unchanged.

The models of the test network, developed in RSCAD are shown in Figure 6 and Figure 7.

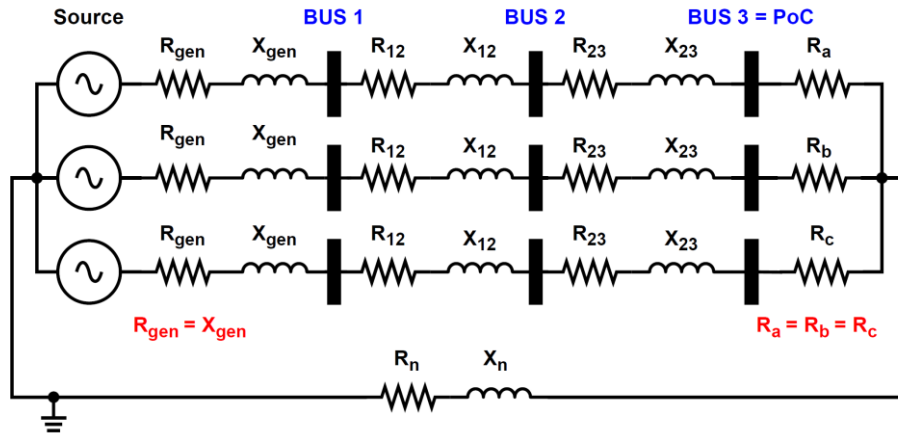


Figure 4: Test A1.1 circuit diagram with source impedance parameters $R_{gen} = X_{gen} = 0.2645 \Omega$, transmission line parameters $R_{12} = X_{12} = 0.2116 \Omega$, $R_{23} = X_{23} = 0.3174 \Omega$, $R_n = X_n = 0.5290 \Omega$, and load parameters $R_a = R_b = R_c = 7.9350 \Omega$. The source voltage was initialised to 254.0430 V with phase A voltage angle = 5.1944°

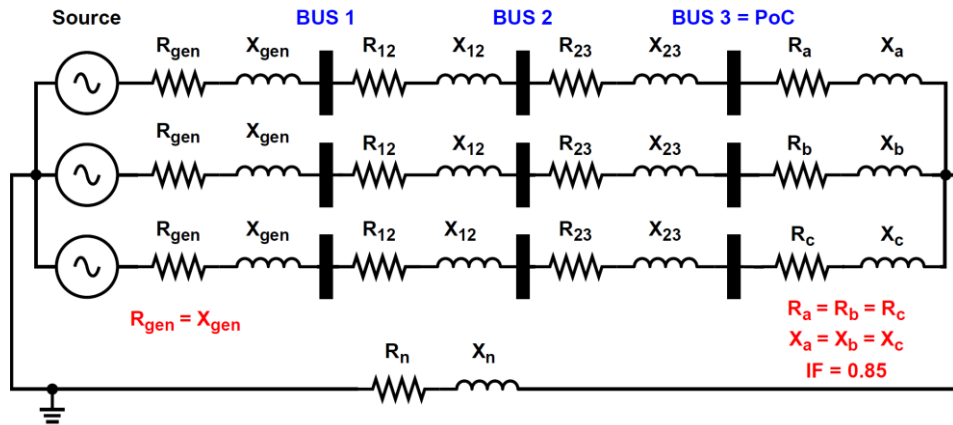


Figure 5: Test A1.2 circuit diagram with same parameters as Test A1.1 except for load parameters $R_a = R_b = R_c = 5.7330 \Omega$ and $X_a = X_b = X_c = 3.5530 \Omega$.

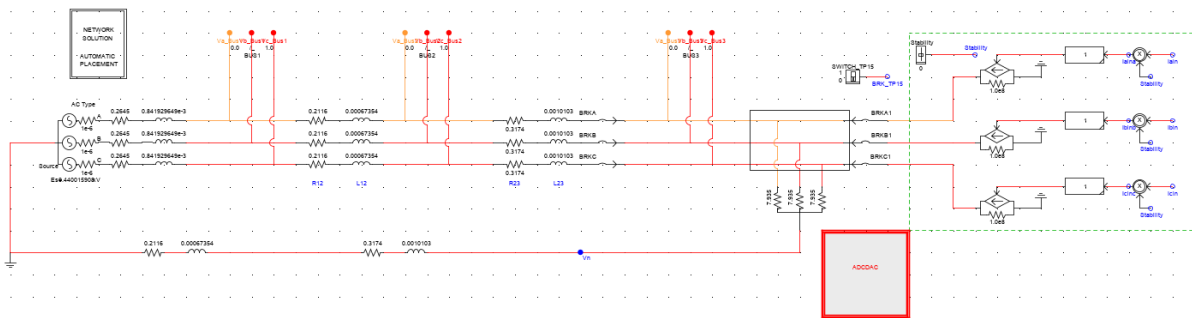


Figure 6: Test A1.1 circuit modelled in RSCAD. The software blocks used to interface the real-time simulated model and the 10 kW converter through the power amplifier is shown by current

sources on the right of the diagram.

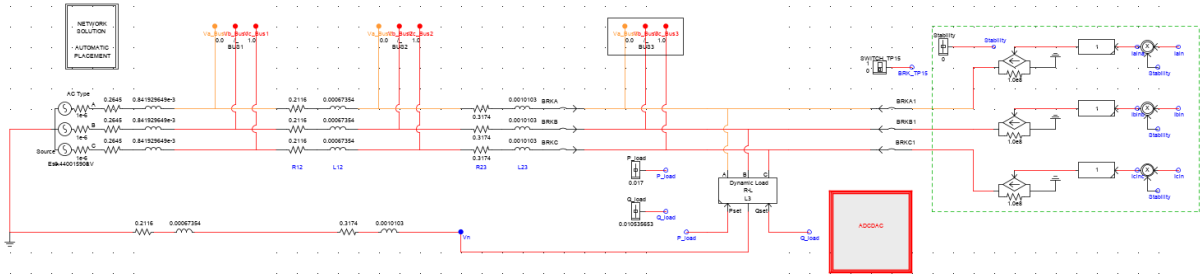


Figure 7: Test A1.2 circuit modelled in RSCAD. The software blocks used to interface the real-time simulated model and the 10 kW converter through the power amplifier is shown by current sources on the right of the diagram.

3.2.2 Additional PHIL Tests at DPSL

Figure 8 shows the base case test network which was developed using a 20 kW load with 10 % or 2 kW power delivery loss.

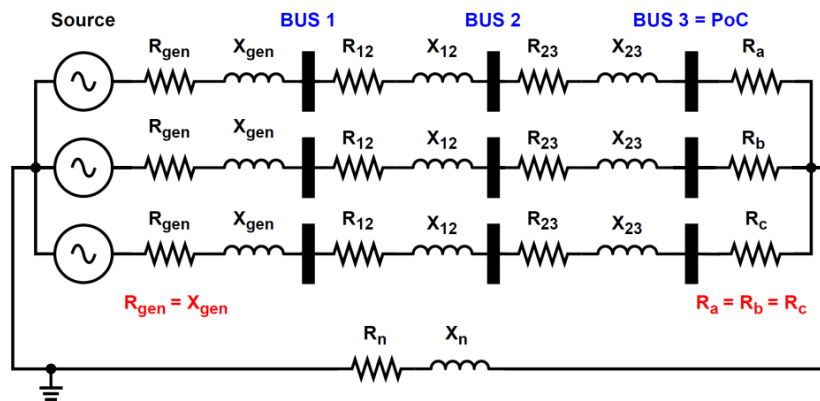


Figure 8: Test 1 circuit diagram with source impedance parameters $R_{gen} = X_{gen} = 0.2645 \Omega$, transmission line parameters $R_{12} = X_{12} = 0.2116 \Omega$, $R_{23} = X_{23} = 0.3174 \Omega$, $R_n = X_n = 0.5290 \Omega$, and load parameters $R_a = R_b = R_c = 7.9350 \Omega$. The source voltage was initialised to 254.0430 V with phase A voltage angle = 5.1944°

Figure 9 shows the base case test network which was developed using a 20 kW resistive and inductive load with an impedance factor of 0.85. The transmission line impedance and generator impedance were kept the same as in test 1. The generator terminal voltage was also left unchanged.

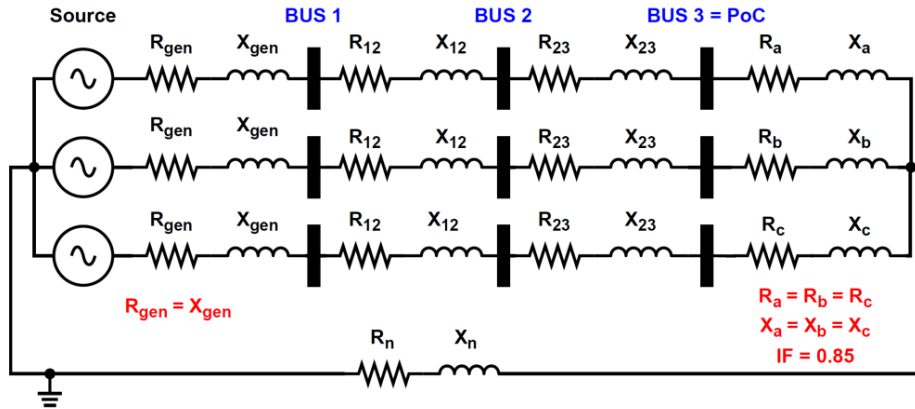


Figure 9: Test 2 circuit diagram with source impedance parameters $R_{gen} = X_{gen} = 0.2645 \Omega$, transmission line parameters $R_{12} = X_{12} = 0.2116 \Omega$, $R_{23} = X_{23} = 0.3174 \Omega$, $R_n = X_n = 0.5290 \Omega$, and load parameters $R_a = R_b = R_c = 5.7330 \Omega$ and $X_a = X_b = X_c = 3.5530 \Omega$. The source voltage was initialised to 254.0430 V with phase A voltage angle = 5.1944°

The same test model shown in Figure 8 was used for test 3 but with a different set of network parameters. The network was designed using a 25 kW load with 10 % or 2.5 kW power delivery loss.

For test 4, due to instability issues experienced with the PHIL test bed with high inductances in the circuit, the following changes were made to the model of test 3:

1. The source inductance from test 3 was removed. Therefore, the Thevenin equivalent of the network shown in Figure 9 was changed as follows to $R_{th} = 0.48 \Omega$ and $X_{th} = 1.92 \Omega - 1.2 \Omega = 0.72 \Omega$.
2. The load parameters were changed to $R_a = R_b = R_c = 3.468 \Omega$ and three load inductances $L_a = L_b = L_c = 1 \text{ mH}$ were added in series to the load resistors. Using a more inductive load introduced instability in the simulation even without any current injection. It appeared that the PHIL test bed was unstable for highly inductive circuits.

The source voltage was left unchanged at $(V_{th})_{ph} = 234.0939982 \angle 19.98310653^\circ$

Due to instability issues experienced with the PHIL test bed with high unbalance in the circuit, a test circuit was developed for small voltage unbalance at the PoC. This was test 5 of the series of additional tests carried out at DPSL. The test circuit was designed as follows:

1. The source impedance was removed. Therefore, the Thevenin equivalent of the network was changed to $R_{th} = 0.48 \Omega$ and had an X/R ratio of 1 (so $X_{th} = 0.48 \Omega$).
2. The load on phases A, B and C were set to 10 kW, 9 kW and 9.5 kW respectively with an impedance factor of 1 and a PoC voltage of 200 V. Therefore, the load resistances were set to $R_a = 4.0000 \Omega$, $R_b = 4.4444 \Omega$ and $R_c = 4.2105 \Omega$.

The source voltage was left unchanged at $(V_{th})_{ph} = 234.0939982 \angle 19.98310653^\circ$

The hardware-in-the-loop test bed is shown in Figure 10. It consists of the Real Time Digital Simulator (RTDS) which sends instantaneous voltages and currents measured at the PoC to the Triphase 10 kW converter controller. The measured voltages and currents were exported as a .csv file which was then read in MATLAB. The measured quantities were converted to a timeseries such that a Discrete Fourier Transform could be implemented to extract the CRMS values of voltages and currents including their angles with respect to the reference phasor \mathbf{V}_{AN} . The calculated CRMS values and calculated Thevenin Equivalent Impedance of the network from the PoC were input to a GPT spreadsheet which gives as outputs, the reference

compensating currents to be injected by the 10 kW converter. The reference currents were then specified within the GPT-based current control algorithm. The uncompensated system was allowed to run on the RTDS until steady state was reached. Then, the converter currents were slowly ramped in and injected into the simulated test network through the Triphase 90 kVA converter which acts as a power amplifier.

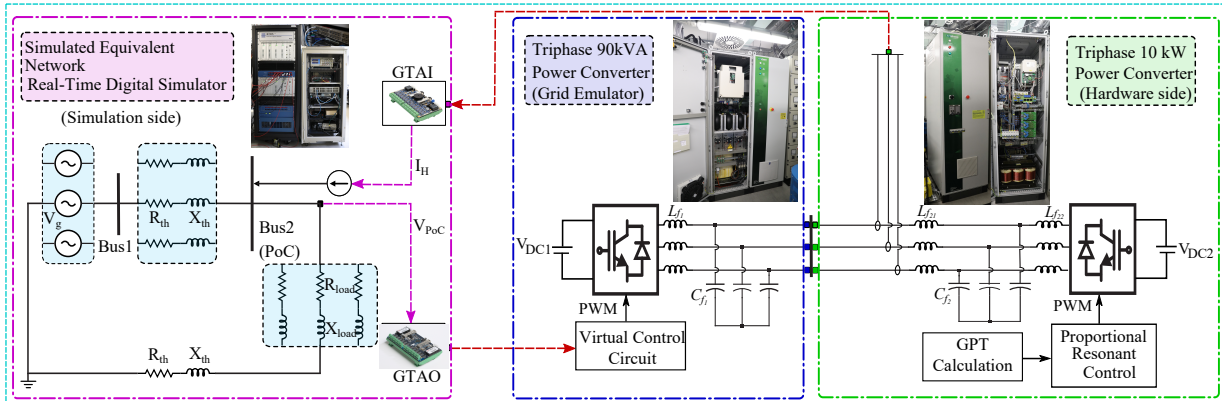


Figure 10: Hardware-In-the-Loop test bed

Figure 11 shows a photo of the control room where we monitored the controller signals, measured quantities from the HIL testbed including the RSCAD simulation model quantities.



Figure 11: Photo of control room with multiple screens to monitor parameters and measured quantities in the 10 kW converter controller, RSCAD simulation model, the dc-power source and 90 kVA power amplifier. The 10 kW converter and 90 kVA power amplifier can also be observed in the experimental testing room.

3.2.3 Real-lab Tests at PNDC

The circuit configuration at PNDC is shown in Figure 12. For the tests, the network was reconfigured to a three-phase, three-wire power system. The whole network's infeed is supplied by the local distribution network operator. A 2 MVA 11/11 kV Dyn11 isolation

transformer supplies the primary switchboard (SWB). The MV network consists of 130 m of 11 kV, 95 mm² copper XLPE cables (MV-007 and MV-013), and a mock impedance unit (MIU1). The MV network supplies different substations easily added or removed from the network. In this case, substation A was chosen for the tests since the transformer (GMU-A) is rated 315 kVA, 11/0.433 kV, Dyn11. The primary windings of GMU-A were connected to bus 0. The secondary windings of GMU-A were connected to bus 1. The LV cables run from bus 1 to bus 3 and are labelled on Figure 12. For example, buses 1 and 2 are connected through 260 m of LV 185 mm² copper XLPE cables (LV 001 to LV 004). Buses 2 and 3 are connected through 455 m of the 185 mm² copper XLPE cables (LV 005, LV 014, LV 021, LV 022, LV 023). Load banks, shown in green in Figure 12 are connected at bus 3. All loads downstream of bus 3 are treated as a lumped system load. Test bays are shown in red. A regenerative three-phase load emulator was connected to test bay F1 at bus 2. It acts both as a current source and/or current sink. In some tests, the load emulator was moved to test bay B1, downstream bus 3. The GPT-controlled compensator was connected to test bay D1 at bus 3. The dc-bus of the converter was supplied by two parallel 18 kW, 400 V dc-power supplies.

Unbalance was introduced by either changing the load configurations or using a regenerative three-phase load emulator capable of simultaneously drawing or injecting currents. Harmonics were also injected or drawn using the load emulator.

Measurements were made using Fluke meters installed at test bay D1, F1 and F2. An uncalibrated Beckhoff Data Acquisition System was used at test bay D1 to measure the PoC voltages and currents for post-processing. Table 7 shows the position of the fluke meters with respect to the network diagram in Figure 12, measurements made at each bus and the position of the Fluke current clamps for current measurement on specific cables within the network.

Table 7: Position of meters for tests at PNDC

Designation	Measurements made	Cable used for current measurement
Fluke F2	Bus 1 voltages and currents	LV 002
Fluke F1	Bus 2 voltages and currents	LV 005
Fluke D1	Inverter output currents Bus 3 voltage	Inverter ac connections
Beckhoff D1	Bus 3 voltages and currents	LV 021

The Low Voltage (LV), Medium Voltage (MV) and High Voltage (HV) network diagrams were provided by PNDC. Underground cable datasheets including lengths were also provided with the aim of determining the Thévenin-Equivalent Impedance (TEI) of the network. The TEI serves as an input to the calculation of compensating currents using the GPT approach.

The Thévenin Equivalent Impedance from the equivalent source to Test Bay D2 (Bus 3) was calculated to be $R = 0.1741 \Omega/\text{phase}$ and $X = 0.09954 \Omega/\text{phase}$

400 Vac, 3-ph, operated as 3-wire microgrid

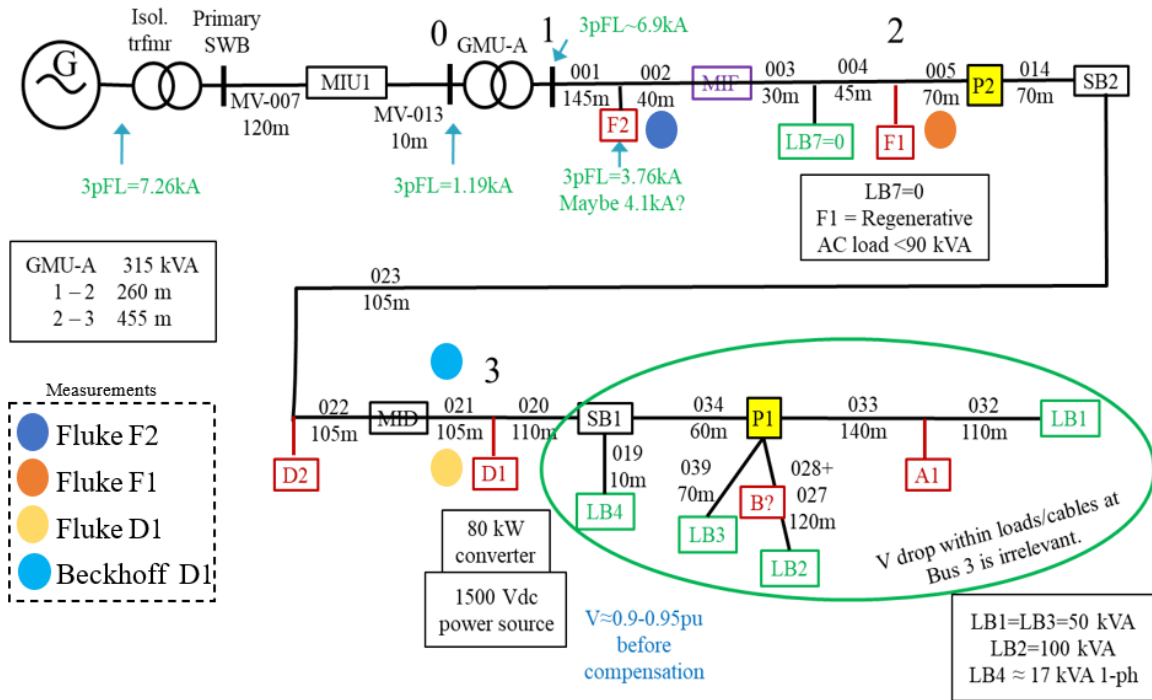


Figure 12: Connection diagram of test system at PNDC.

The 80 kW converter specifications are shown in Table 8. Images of the step down GMU-A transformer, LV cables, one of the load banks and their location on a one-line diagram of the network are shown in Figure 13. A photograph of the converter being connected to test bay D1 is shown in Figure 14.

Table 8: Specifications of the 80 kW inverter used in PNDC

Manufacturer	ArioGenix, South Africa
Serial number	0501000C
Configuration	3-phase, 3-wire, Active Neutral Point Clamped (ANPC)
Rated voltage	400 - 690 Vac, 1500 Vdc (max)
Rated power	80 kW
DC bus capacitance	1.4 mF (each)
Inverter-side filter inductance	370 μH
Grid-side filter inductance	192 μH
Filter capacitance	28 μF (Δ connected)
Switching frequency	8275 Hz
Sampling frequency	13 kHz

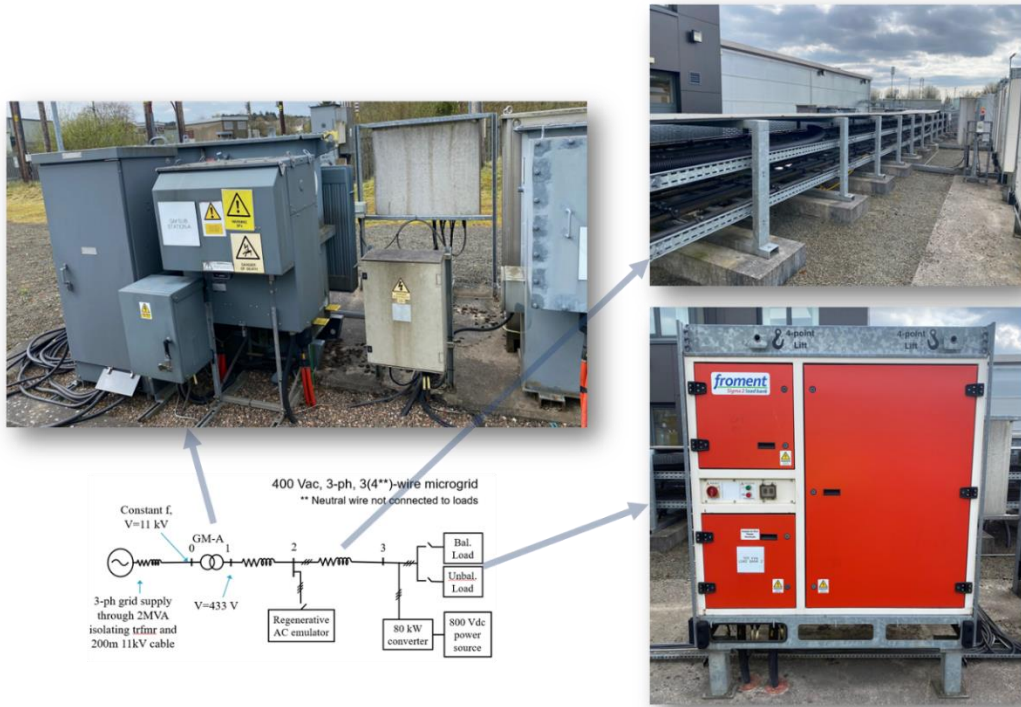


Figure 13: Photograph of 315 kVA 11/0.433 kV GMU-A step down transformer, LV cables, and load bank LB2

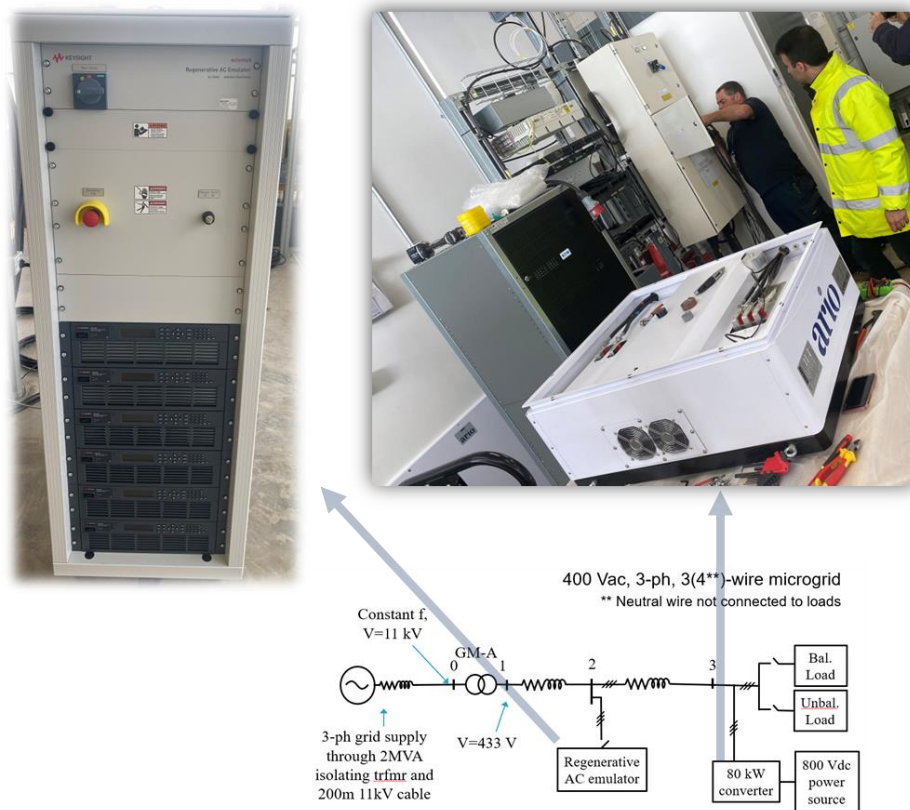


Figure 14: Photographs of 80 kW converter being connected to test bay D1 and regenerative controllable load

For each test case, the following procedures were adopted:

1. Ensure that the 80-kW power converter is off and in “Safety mode”.
2. Set the HV network live (task carried out by an HV-certified engineer).
3. Switch on the load banks used in the test manually (task carried out by certified engineer).
4. Using the load bank software tool available at PNDC, set the total load apparent power and power factor settings.
5. Using the load bank software tool, close the load isolators to switch in the load on the network.
6. Run the power system network for 10 minutes to ensure that that steady state is reached, and the voltages and currents observed are sensible.
7. Ensure all Fluke meters are synchronised in date and time.
8. Using the Fluke meter and Beckhoff Data Acquisition System, start measurements of the voltages and currents. Record the measurements for 1 minute.
9. Using the load bank software, switch off all loads. The HV network can still be kept live but no current flows in the network due to a no-load condition.
10. Collect the PoC measurements from the Beckhoff Data Acquisition System and save as a .csv file.
11. Post-process the measurements by performing a Fast-Fourier Transform (FFT) and calculating the complex RMS (CRMS) values of currents and voltages for each harmonic frequency. Enter the CRMS values and angles on a GPT spreadsheet.
12. Enter the Thévenin-equivalent impedance calculated using network reduction onto the GPT spreadsheet. Generate the compensating current references for the converter. Note that all angles for the compensating currents calculated on the GPT spreadsheet must be referenced with respect to the reference vector VBA after compensation. Hence, the angle of vector VBA after compensation was subtracted from each calculated angle of the compensating currents.
13. Using Code Composer Studio, initialize the converter controller by entering the magnitude and angle values of the compensating current components for each harmonic frequency.
14. Compile the control code and switch on the converter. The converter can be switched on by increasing the dc-bus voltage to 400 V using the dc-power supply.
15. Using the load bank software tool, close the load isolators to switch on the loads.
16. Wait for 2-3 minutes to allow the network to reach steady state.
17. Using the Fluke meters and Beckhoff Data Acquisition System, start measurements of the voltages and currents. Start a stopwatch.
18. After 60 s, remove “Safety mode” and enable the inverter by connecting to its user-interface. After synchronising to the PoC voltage, the contactor between the converter and the PoC closes. The converter now forms part of the network and injects compensating currents calculated by the GPT.
19. Allow the converter to run for at least 90 s and disable the converter using its user interface. The converter is now not connected to the network.

20. Let the system run without the converter for 60 s and then turn off all loads.
21. Repeat steps 4 to 20 for each test case.

3.3 Data Management and Processing

3.4 Description of measurement systems at PNDC

The following meters were used at PNDC to collect measurements at buses 1 to 3:

- Fluke 430 Series II Power Quality and Energy Analysers
The "Power Wave" function of Fluke 435 II Power Quality Analysers was used to record the instantaneous values of voltage and current signals at less than 4 kHz sampling frequency.
- Beckhoff Data Acquisition System
The analogue input cards EL3783 and EL3104 of Beckhoff system were used to record the instantaneous values of voltage and current signals, respectively. The sampling frequency was set to 5 kHz.

3.4.1 Extracting data from Fluke and Beckhoff Data Acquisition Systems

The Fluke meters are equipped with in-built calculations of rms values, THD, harmonic spectrum, statistical data representation amongst other functionalities. However, the calculation steps are not specified in the Fluke meter user guide. Therefore, it was preferred to extract instantaneous values of currents and voltages measured by each Fluke meter and post-process the data to analyse the results. The Fluke meter exports data as a .txt file delimited using a tab. For each test case, measurement data was stored on a detachable SD card on the Fluke meter and the .txt file was renamed by assigning a measurement number. The measured data was then copied to a laptop for analysis using PowerLog software and MATLAB Simulink.

The Beckhoff Data Acquisition System was connected at test bay D1 (Bus 3 of the power network). During testing, we needed measurements at the PoC prior to compensation. Measurements were made using the Beckhoff Data Acquisition System and observed in the Beckhoff software on a dedicated laptop. The Beckhoff Data Acquisition System was chosen instead of the Fluke meters since the former can measure at a fixed sampling frequency of 5 kHz. Data from the Beckhoff Data Acquisition System can be exported in different formats. A csv file was preferred in this case as data in a csv file can easily be imported onto MATLAB. The measured data (V_{AB} , V_{BC} , V_{CA} , I_A , I_B , I_C) was then transferred to a USB flash memory and imported on a laptop. A MATLAB script was developed which reads data from the .csv files exported and generates a timeseries for each measured quantity. A Simulink model was then developed which imports the generated timeseries and implements a Discrete Fourier Transform algorithm. The CRMS values of currents and voltages were then used as inputs to the GPT spreadsheet. The outputs were the CRMS values of compensating currents including their angles referenced to the voltage reference phasor. The values of compensating currents were entered manually in the code of the converter controller. This was achieved using Code Composer Studio.

In all test cases, a spreadsheet was used to record the measurement number and the associated dataset was named accordingly. A snippet of the spreadsheet is shown in Table 9.

Table 9: Measurement record on a spreadsheet

ERI-025E Project	Fluke Measurements on Test Bays			
Test Case	Test Bay F1	Test Bay F2	Test Bay D1	Test Bay D1 Beckhoff
C1 - Base	Meas 24			Meas 23
C1 - Test	Meas 28	Meas 28	Meas 28	Meas 28
C2 - Base	Meas 26	Meas 26	Meas 26	Meas 26
C2 - Test	Meas 29	Meas 29	Meas 29	Meas 29

3.4.2 Post-processing of results

Post-processing of the data exported from the Fluke meters and Beckhoff Data Acquisition Systems is discussed in Appendix A, and the time synchronisation method used to align the Beckhoff and Fluke measurements is discussed in Appendix B. Time-synchronisation of Fluke and .

4 Results and Conclusions

4.1 Discussion of Results

We do not present simulations here – they are office work done for the preparation of papers.

For each of the following, we identify the nature of the test, add typical before/with/after compensation figures of waveforms and losses, give (tabulate) the set-up parameters (loads, etc) and calculated results, and interpret the result.

The post-processing used to get the final test results at PNDC is described in Appendix A. The final results are those we use as inputs to simulations and the outputs that we expect to get in the simulations – load currents, voltages before/with/after compensation, losses measured and calculated in the whole and each part of the system, etc.

4.1.1 Test A1.1 at DPSL

Figure 15 shows the PoC voltages and currents for 3 cycles before compensation. The voltages and currents on each wire were in phase with a constant frequency of 50 Hz.

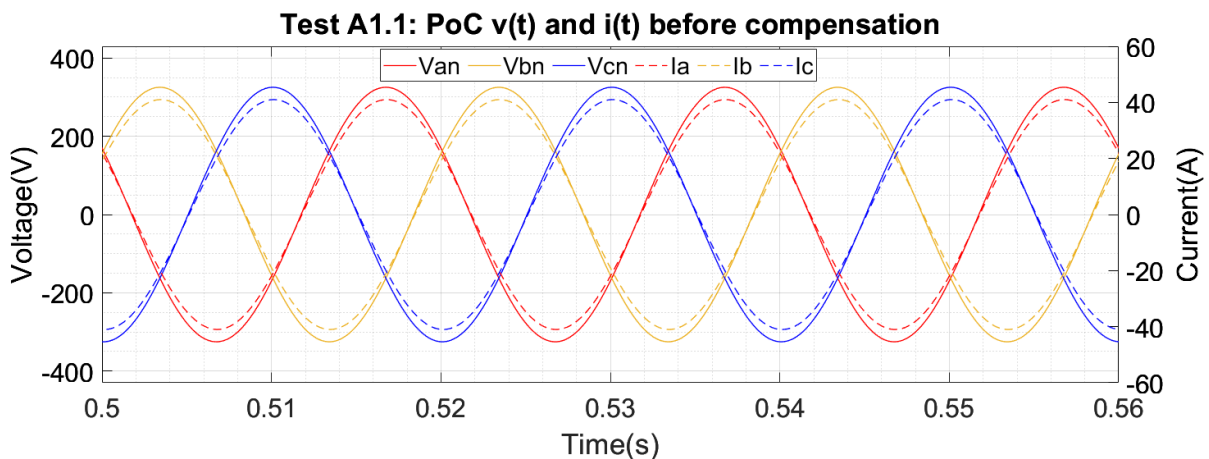


Figure 15: Test A1.1 results showing PoC V and I before compensation.

Using the 3-cycle time interval before compensation, a DFT was implemented on the voltages and currents measured at the PoC. Table 10 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{BA} or V_{21} .

The results before compensation were closely matched between Simulink and RSCAD. Voltages and currents were in phase. It must be noted that, since V_{BA} was chosen as the reference phasor, its angle is always 0. All other angles, for example for the currents, are referenced to the 0.

Table 10: Test A1.1 Inputs to GPT spreadsheet before compensation

System topology inputs			
Freq. components: 1 x Fund. Freq			1
Topology: No. of wires (2 to 5):			4
Dc component (yes=1)			0
Harmonic components (number)			0
INPUTS at PoC		m	Fund. freq h1
			RSCAD
CRMS voltages			$U_{m,h}$ [Vrms], α [deg]
Voltage measure reference wire	1		0.00000 0.00000
	2		230.00000 0.00000
	3		230.00000 -120.00000
	4		230.00000 -240.00000
	0		0.00000 0.00000
CRMS currents			$I_{s m,h}$ [A], α [deg]
If both U and $I=0$: insert $I < 1E-9$ to avoid Div0 condition in calcs	1		0.00000 0.00000
	2		28.98553 0.00000
	3		28.98553 -120.00000
Current unbalance calc below is useful for I in any last wire:	4		28.98553 -240.00000
Current unbalance check	0		0.00000 0.00000
R, X			$r(m,1)$ $r(m,1)$
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with $r=1 \cdot 10^{-8}$ generally ok	1		0.52950 0.52950
	2		0.79350 0.79350
	3		0.79350 0.79350
	4		0.79350 0.79350
	0		0.00000 0.00000

Table 11 shows the GPT-calculated power at the PoC, losses, Thévenin-side power, minimum loss and loss reduction achievable by compensation, the power factor of the whole system which represents the efficiency of power delivery and the apparent power. The calculations validate the model of the test system.

The measured power at the PoC was 20 kW. The delivery losses were 2 kW representing 10 % of the load power. The GPT-calculated power factor of the whole system was 0.9950. The GPT determines that it is possible to further reduce the losses in the delivery system to 1.980 kW by injecting compensating currents shown in Table 12.

Table 11: Test A1.1 Calculated powers, losses, minimum loss, power factor and apparent power before compensation

Calculate power components without compensation	
	RSCAD
Ppoc(h) before opt reassgt	20000.02
Loss $\ I_s'h\ ^2$ (h)	2000.00
Pth(h) before comp	22000.02
Totals	
Tot. Ppoc bef opt reassgt	20000.02
Tot. loss $\ I_s'h\ ^2$ bef opt reass	2000.00
$\ I_s'\ $	44.72
Pth before comp	22000.02
Calculate min. loss, PF and AP	
$\ V_{th}'\ $	493.96
$\ I_A'\ ^2$ (min loss)	1980.00508
PF_{sys} bef comp (by losses)	0.9950
AP_{sys} = $\ I_s'\ \ V_{th}'\ $	22090.74
Loss reduction poss.by comp.	19.998

Table 12: Test A1.1 Calculated optimal compensating currents before compensation

Compensation approach: calculate currents $I_c(m,h)$:		
	lc rms	lc mag
1	0.0000000	-3.6568899
2	2.6243596	-84.2326851
3	2.6243596	155.7673149
4	2.6243596	35.7673149
0	0.0000000	0.00
Check sum I_c		0.0000000

Figure 16 shows the PoC voltages and currents for 3 cycles during compensation. On each wire, the current was lagging the voltage by 6.000° .

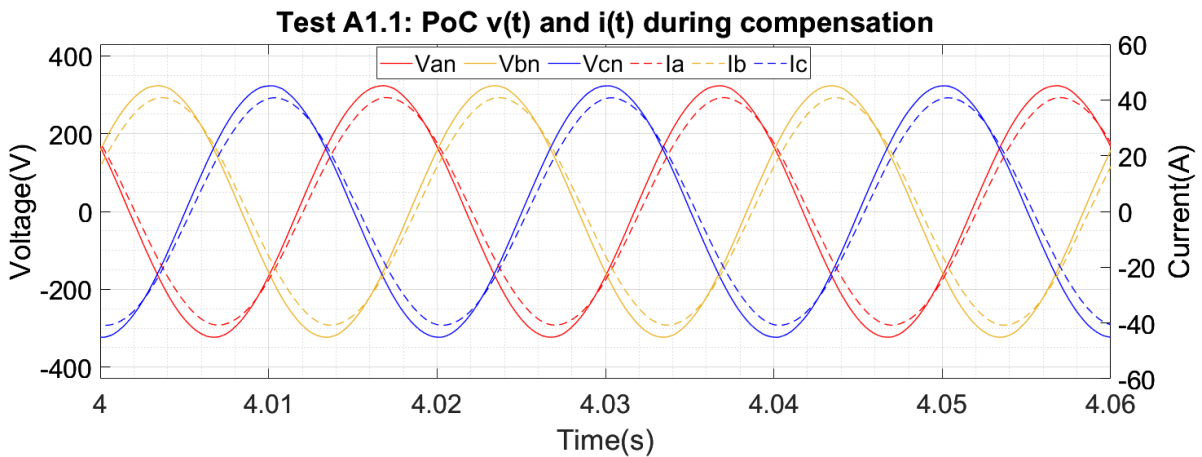


Figure 16: Test A1.1 results showing PoC V and I during compensation.

Using the 3-cycle time interval during compensation, an FFT was implemented on the voltages and currents measured at the PoC. Table 13 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{BA} or V_{21} . The voltage at the PoC dropped as compensating currents were introduced.

Table 13: Test A1.1 Inputs to GPT Spreadsheet during compensation

INPUTS at PoC		m	Fund. freq h1	
			RSCAD	
CRMS voltages			$U_{m,h}$ [Vrms], α [deg]	
Voltage measure reference wire	1	1	0.00000	0.00000
	2	2	228.39493	0.00000
	3	3	228.39395	-120.00000
	4	4	228.39881	-240.00057
	0	0	0.00000	0.00000
CRMS currents			I_s m,h [A], α [deg]	
If both U and $I=0$: insert $I < 1E-9$ to avoid Div0 condition in calcs Current unbalance calc below is useful for I in any last wire: Current unbalance check	1	1	0.00000	0.00000
	2	2	28.80767	-6.00000
	3	3	28.80577	-126.00000
	4	4	28.80564	-245.99000
	0	0	0.00000	0.00000
			-0.00355	-0.00355
R, X			$r(m,1)$	$r(m,1)$
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with	1	1	0.52950	0.52950
	2	2	0.79350	0.79350
	3	3	0.79350	0.79350
	4	4	0.79350	0.79350

r=1*10⁻⁸ generally ok

 | 0 | 0.00000 | 0.00000 |

Table 14 shows the GPT-calculated power at the PoC, losses and Thévenin-side power, the power factor of the whole system and the apparent power. The power at the PoC has dropped by 370 W. The load voltage dropped when compensating currents were injected and so did the delivery losses. The load block in RSCAD appears to behave differently from a constant impedance load although the specified type of load was set “Constant Z”.

The system power factor dropped from 0.9950 to 0.9793. It is still possible to compensate once again and reduce the delivery losses by 80.925 W such that the power factor is improved to unity.

Table 14: Test A1.1 Calculated powers, losses, minimum loss, power factor and apparent power during compensation

Calculate power components	without compensation
	RSCAD
Ppoc(h) before opt reassgt	19629.76
Loss Is'h ² (h)	1975.35
Pth(h) before comp	21605.11
Totals	
Tot. Ppoc bef opt reassgt	19629.76
Tot. loss Is' ² bef opt reass	1975.35
Is'	44.44
Pth before comp	21605.11
Calculate min. loss, PF and AP	
Vth'	494.52
Ia' ² (min loss)	1894.42851
PF _{sys} bef comp (by losses)	0.9793
AP _{sys} = Is' Vth'	21979.11
Loss reduction poss.by comp.	80.925

Figure 17 shows the PoC voltages and injected compensating currents using a physical 10 kW converter retrofitted with GPT control.

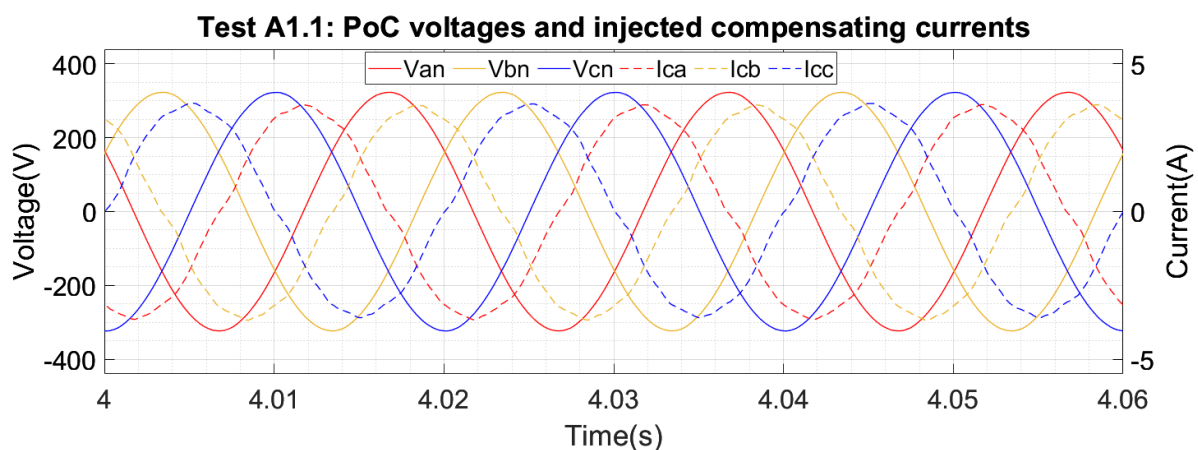


Figure 17: Test A1.1 results showing PoC V and injected compensating I during compensation

The injected compensating currents from the 10 kW converter were distorted with harmonics. The dominant harmonics were the 3rd, 5th, 7th, 11th, and 13th, typical of most power-electronic converters running below rated conditions. Experience with testing converters at currents much below their rated values has shown that the currents become distorted with harmonics

since the IGBTs do not operate at rated conditions. The 10 kW converter was designed to operate at rated current equal to 21.7 A. In test A1.1, the converter only injected 2.56 A rms compensating currents in each phase as shown in Table 15. This resulted in harmonic distortion of the compensating currents.

More importantly, Table 15 shows that the angles of the injected fundamental frequency compensating currents did not match the angles of their reference currents. This problem was tracked back as follows:

Measurements of the reference current and injected compensating currents from the converter were made in two ways: first using MATLAB Simulink and secondly from the RTDS. Table 15 shows the results from measured RTDS data. In this case, the injected currents did not match the reference currents. When an FFT was done using measurements from MATLAB Simulink, it was observed that the reference currents and injected currents were closely matched. We observed that the RTDS data was not captured long enough. During the 5-s captured data the system had not settled to steady-state. The Simulink data was captured for a longer time than the RTDS data and included the steady-state condition whereby the converter reference currents and injected currents were matched.

Table 15: Test A1.1 Fundamental frequency reference and injected compensating currents

Phase	Ref rms	Ref angle	Injected rms	Injected angle
A	2.6243933	-84.2326463	2.5588735	-271.0564939
B	2.6243931	155.7673566	2.5617023	-31.0590440
C	2.6243919	35.7673600	2.5578371	-151.1010370

4.1.2 Test A1.2 at DPSL

Figure 18 shows the PoC voltages and currents for 3-cycles before compensation. The current was lagging the voltage by 32.689° .

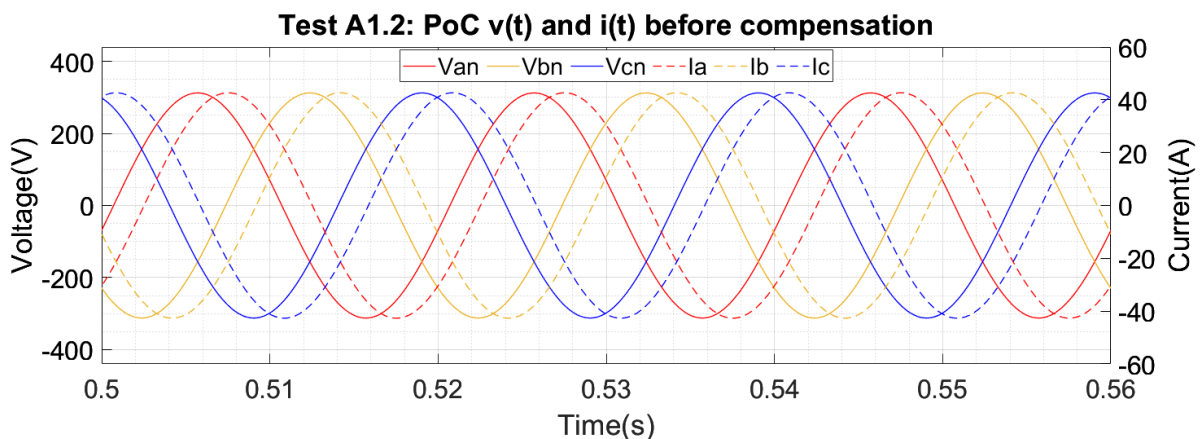


Figure 18: Test A1.2 results showing PoC V and I before compensation

Table 16 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{BA} or V_{21} . Table 17 shows the power components calculated by the GPT. The power delivered to the load at bus 3 was 16.832 kW. Table 18 shows the calculated compensating currents.

Table 16: Test A1.2 Inputs to GPT Spreadsheet before compensation

INPUTS at PoC		m	Fund. freq h1	
CRMS voltages			RSCAD	
			Um,h [Vrms], α [deg]	
Voltage measure reference wire		1	0.00000	0.00000
		2	220.96447	220.96447
		3	220.96459	220.96459
		4	220.96450	220.96450
		0	0.00000	0.00000
CRMS currents			Is m,h [A], α [deg]	
If both U and I=0: insert I<1E-9 to avoid Div0 condition in calcs		1	0.00000	0.00000
		2	30.17061	30.17061
		3	30.17060	30.17060
Current unbalance calc below is useful for I in any last wire:		4	30.17061	30.17061
Current unbalance check		0	0.00000	0.00000
R, X			r(m,1)	r(m,1)
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with r=1*10^-8 generally ok		1	0.52950	0.52950
		2	0.79350	0.79350
		3	0.79350	0.79350
		4	0.79350	0.79350
		0	0.00000	0.00000

Table 17: Test A1.2 Calculated powers, losses, minimum loss, power factor and apparent power before compensation

Calculate power components without compensation	
	RSCAD
Ppoc(h) before opt reassgt	16832.23
Loss Is'h ^2 (h)	2166.89
Pth(h) before comp	18999.12
Totals	
Tot. Ppoc bef opt reassgt	16832.23
Tot. loss Is' ^2 bef opt reass	2166.89
Is'	46.55
Pth before comp	18999.12
Calculate min. loss, PF and AP	
Vth'	494.16
IA' ^2 (min loss)	1354.47026
PFsys bef comp (by losses)	0.7906
APsys= Is' Vth'	23003.15
Loss reduction poss.by comp.	812.417

Table 18: Test A1.2 Calculated optimal compensating currents before compensation

Compensation approach: calculate currents Ic(m,h):		RSCAD	
		Ic rms	Ic angle
	1	0.00	-77.45
	2	17.04246	-84.78760
	3	17.04247	155.21238
	4	17.04246	35.21242
	0	0.00	0.00
	Check sum Ic	0.00	

Figure 19 shows the PoC voltages and currents for 3-cycles during compensation. The phase shift between currents and voltages decreased. The voltages and currents in the PHIL test bed are slightly distorted which shows that PHIL tests provide a more representative effect of compensation using a power-electronic converter compared to a controlled current source.

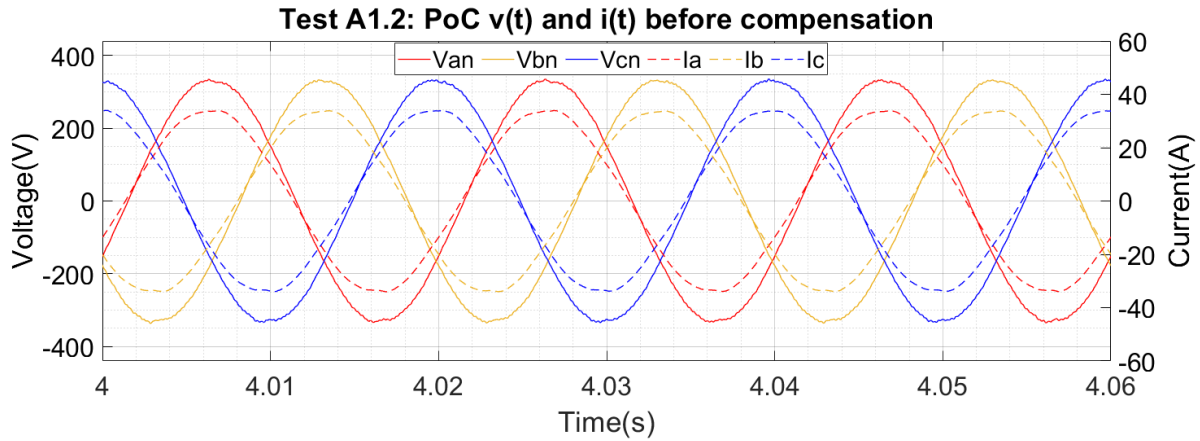


Figure 19: Test A1.2 results showing PoC V and I during compensation

Table 19 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{BA} or V_{21} . The voltage at the PoC increased upon injection of the compensating currents. Table 20 shows that the power factor was improved from 0.7906 to 0.9997 by GPT-compensation. The power consumed by the load increased showing the effect of the constant impedance load to an increase in voltage. The power system model has become more efficient in delivering power when compensation is introduced and the losses have reduced from 812 W.

Table 19: Test A1.2 Inputs to GPT Spreadsheet during compensation

INPUTS at PoC		m	Fund. freq h1	
			RSCAD	
CRMS voltages			Um,h [Vrms], α [deg]	
Voltage measure reference wire	1	0.00000	0.00000	
	2	235.48620	235.48620	
	3	235.50844	235.50844	
	4	235.48967	235.48967	
	0	0.00000	0.00000	
CRMS currents			Is m,h [A], α [deg]	
If both U and I=0: insert <1E-9 to avoid Div0 condition in calcs	1	0.00000	0.00000	
	2	24.11766	24.11766	
	3	24.12802	24.12802	
	4	24.13855	24.13855	
	0	0.00000	0.00000	
Current unbalance calc below is useful for I in any last wire: Current unbalance check			0.00000	0.00000
R, X			r(m,1) r(m,1)	
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with r=1*10^-8 generally ok	1	0.52950	0.52950	
	2	0.79350	0.79350	
	3	0.79350	0.79350	
	4	0.79350	0.79350	
	0	0.00000	0.00000	

Table 20: Test A1.2 Calculated powers, losses, minimum loss, power factor and apparent power during compensation

Calculate power components with compensation	
	RSCAD
Ppoc(h) before opt reassgt	17019.47
Loss $\ I_s'h\ ^2$ (h)	1385.84
Pth(h) before comp	18405.31
Totals	
Tot. Ppoc bef opt reassgt	17019.47
Tot. loss $\ I_s'\ ^2$ bef opt reass	1385.84
$\ I_s'\ $	37.23
Pth before comp	18405.31
Calculate min. loss, PF and AP	
$\ V_{th}'\ $	494.55
$\ I_A'\ ^2$ (min loss)	1384.93765
PF _{SYS} bef comp (by losses)	0.9997
AP _{SYS} = $\ I_s'\ \ V_{th}'\ $	18410.42
Loss reduction poss.by comp.	0.904

PoC voltages and compensating currents injected are shown in Figure 20. Table 21 tabulates the reference and the injected compensating currents' rms and angle. The converter injected currents with small steady-state errors of around 2.5 %.

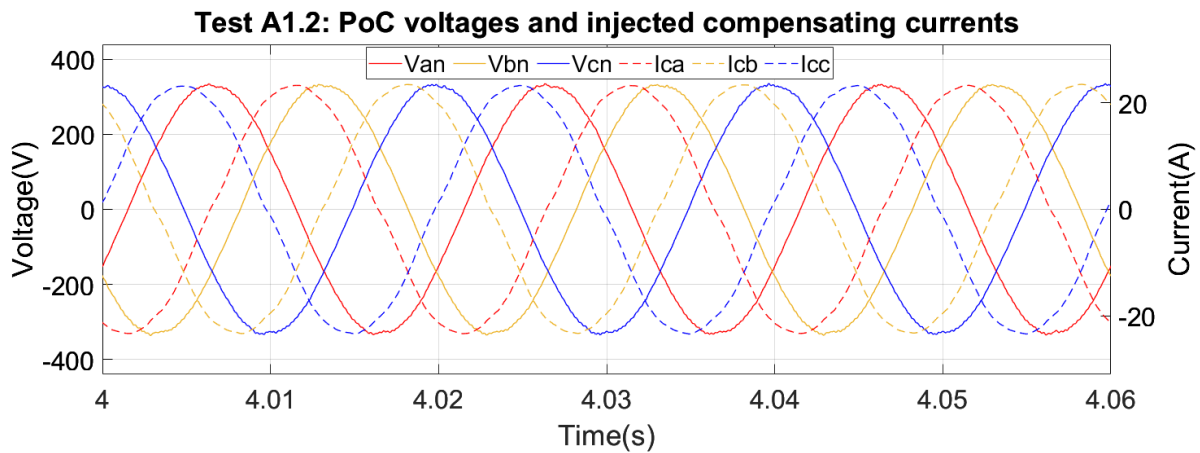


Figure 20: Test A1.2 results showing PoC V and injected compensating I during compensation

Table 21: Test A1.2 Fundamental frequency reference and injected compensating currents

Phase	Reference		Injected	
	rms	angle	rms	angle
A	17.04246	-84.78760	16.61544	-89.01308
B	17.04247	155.21238	16.64602	151.0120
C	17.04246	35.21242	16.63207	30.92280

4.1.3 Additional test A1 at DPSL

Figure 21 and Figure 22 show the PoC voltages and currents for 3-cycles before compensation in Simulink and RSCAD respectively. In both cases, the voltages and currents on each wire were in phase with a constant frequency of 50 Hz.

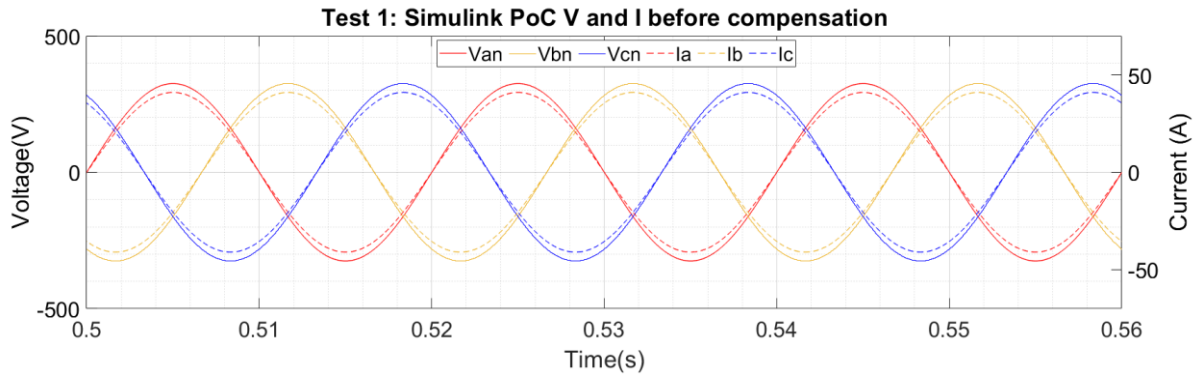


Figure 21: Test 1 Simulink results showing PoC V and I before compensation.

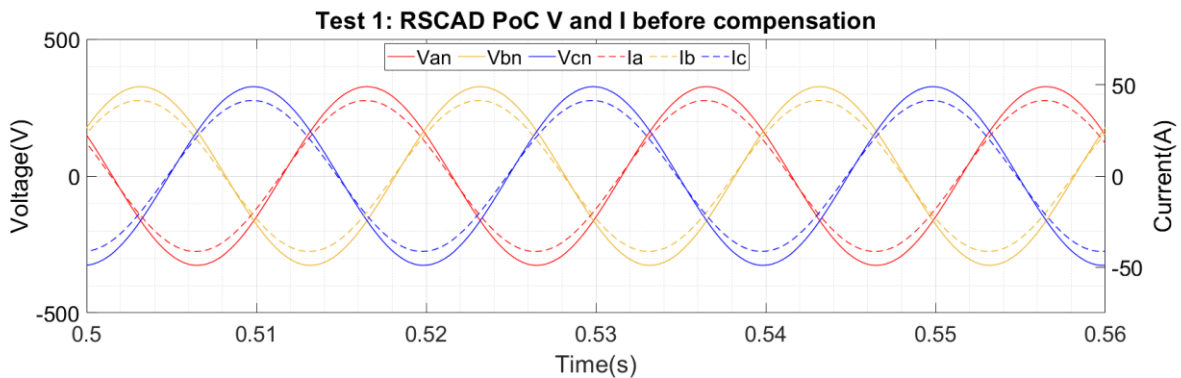


Figure 22: Test 1 RSCAD results showing PoC V and I before compensation.

Using the 3-cycle time interval before compensation, a Discrete Fourier Transform (DFT) was implemented on the voltages and currents measured at the PoC. Table 22 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{AN} or V_{21} .

The results before compensation were closely matched between Simulink and RSCAD. Voltages and currents were in phase at the PoC. It must be noted that, since V_{AN} was chosen as the reference phasor, its angle is always 0. All other angles, for example for the currents, are referenced to the 0.

Table 23 shows the GPT-calculated power at the PoC, losses, Thévenin-side power, minimum loss and loss reduction achievable by compensation, the power factor of the whole system which represents the efficiency of power delivery and the apparent power. The calculations validate the model of the test system.

In both RSCAD and Simulink, the measured power at the PoC was 20 kW. The delivery losses were 2 kW representing 10 % of the load power. The GPT-calculated power factor of the whole system was 0.9950. The GPT determines that it is possible to further reduce the losses in the delivery system to 1.980 W by injecting compensating currents shown in Table 24. Negligible differences were observed in the calculated compensating currents from the Simulink and RSCAD simulations.

Table 22: Test 1 Inputs to GPT Spreadsheet before compensation

System topology inputs				
Freq. components: 1 x Fund. Freq		1		
Topology: No. of wires (2 to 5):		4		
Dc component (yes=1)		0		
Harmonic components (number)		0		
INPUTS at PoC	m	Fund. freq h1		
		MATLAB		RSCAD
		Um,h [Vrms], α [deg]		Um,h [Vrms], α [deg]
CRMS voltages				
Voltage measure reference wire	1	0.00000	0.00000	0.00000
	2	229.99982	0.00000	230.00000
	3	229.99982	-120.00000	230.00000
	4	229.99982	120.00000	230.00000
	0	0.00000	0.00000	0.00000
CRMS currents		Is m,h [A], α [deg]		Is m,h [A], α [deg]
If both U and I=0: insert $1E-9$ to avoid Div0 condition in calcs	1	0.00000	0.00000	0.00000
	2	28.98571	0.00000	28.98553
	3	28.98571	-120.00000	28.98553
Current unbalance calc below is useful for I in any last wire: Current unbalance check	4	28.98571	120.00000	28.98553
	0	0.00000	0.00000	0.00000
		0.00000	-145.03596	0.00000
R, X		r(m,1)	x(m,1)	r(m,1)
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with $r=1*10^{-8}$ generally ok	1	0.52950	0.52950	0.52950
	2	0.79350	0.79350	0.79350
	3	0.79350	0.79350	0.79350
	4	0.79350	0.79350	0.79350
	0	0.00000	0.00000	0.00000

Table 23: Test 1 Calculated powers, losses, minimum loss, power factor and apparent power before compensation

Calculate power components without compensation		
	MATLAB	RSCAD
Ppoc(h) before opt reassgt	20000.13	20000.02
Loss $\ Is'h\ ^2$ (h)	2000.03	2000.00
Pth(h) before comp	22000.16	22000.02
Totals		
Tot. Ppoc bef opt reassgt	20000.13	20000.02
Tot. loss $\ Is'\ ^2$ bef opt reass	2000.03	2000.00
$\ Is'\ $	44.72	44.72
Pth before comp	22000.16	22000.02
Calculate min. loss, PF and AP		
$\ Vth'\ $	493.96	493.96
$\ I_A'\ ^2$ (min loss)	1980.02999	1980.00508
PF _{sys} bef comp (by losses)	0.9950	0.9950
AP _{sys} = $\ Is'\ \ Vth'\ $	22090.88	22090.74
Loss reduction poss.by comp.	19.999	19.998

Table 24: Test 1 Calculated optimal compensating currents before compensation

Compensation approach: calculate currents I _c (m,h):		MATLAB		RSCAD	
		Ic rms	Ic angle	Ic rms	Ic angle
	1	3.71145	-84.23265	3.71140	-84.23269
	2	3.71145	155.76736	3.71140	155.76731
	3	3.71145	35.76736	3.71140	35.76731

Figure 23 and Figure 24 show the PoC voltages and currents for 3-cycles during compensation in Simulink and RSCAD respectively. Differences were observed in the results collected from

both software. In Simulink, on each wire, the current was leading the voltage by 5.152° . In RSCAD, on each wire, the current was leading the voltage by 3.990° .

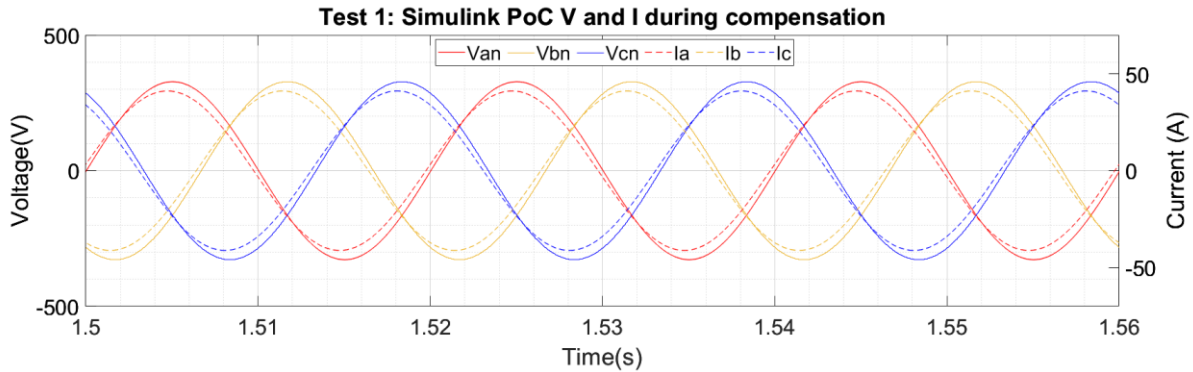


Figure 23: Test 1 Simulink results showing PoC V and I during compensation

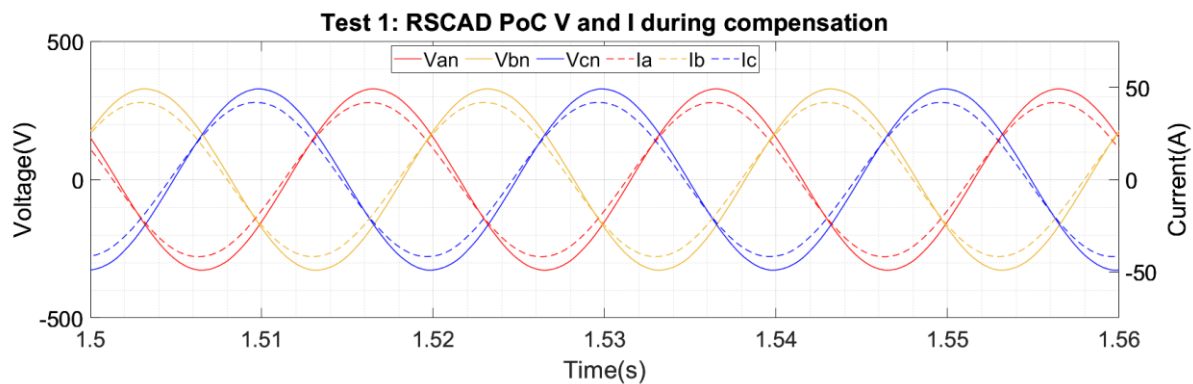


Figure 24: Test 1 RSCAD results showing PoC V and I during compensation

Using the 3-cycle time interval during compensation, a DFT was implemented on the voltages and currents measured at the PoC from both software. Table 25 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{AN} or V_{21} . The differences between in MATLAB and RSCAD are evident from Table 25. The load's response to the increase in voltage during compensation appears different in Simulink and RSCAD although both adopt the model of a constant impedance load. Simulink shows a higher PoC voltage than RSCAD. The phase shift between voltages and currents also differs in software. This highlights an important finding: PHIL tests are highly dependent on the model of the power system equipment available in the software library. Some blocks may not always correctly reproduce a power system's response.

Table 26 shows the GPT-calculated power at the PoC, losses, Thévenin-side power, the power factor of the whole system and the apparent power. In Simulink, the power at the PoC has increased by 152.53 W during compensation. In RSCAD, the power at the PoC increased by 485.40 W. It appears that the constant impedance load responses to the change in voltage during compensation in MATLAB and RSCAD were different.

Simulink showed that the delivery losses increased by 13.89 W with compensation. This is because the voltage at the PoC increased during compensation. The constant-impedance resistive load dissipated more heat, therefore consumed more power or current. In RSCAD, the same effects were observed but with higher power losses due to the higher load.

Simulink showed that the power factor was improved to unity by compensation using the GPT and that no further compensation of the system was required. RSCAD showed that the power factor increased from 0.9950 to 0.9995. In both software, injection of the GPT calculated

currents improved the efficiency of power delivery.

Table 25: Test 1 Inputs to GPT Spreadsheet during compensation

INPUTS at PoC		m	Fund. freq h1			
CRMS voltages			MATLAB		RSCAD	
			Um,h [Vrms], α [deg]		Um,h [Vrms], α [deg]	
Voltage measure reference wire	1	1	0.00000	0.00000	0.00000	0.00000
	2	2	231.89042	0.00000	231.38520	0.00000
	3	3	231.89027	-119.99993	231.38393	-120.00010
	4	4	231.89058	120.00006	231.38469	-239.99933
	0	0	0.00000	0.00000	0.00000	0.00000
CRMS currents			/s m,h [A], α [deg]		/s m,h [A], α [deg]	
If both U and I=0: insert <1E-9 to avoid Div0 condition in calcs Current unbalance calc below is useful for I in any last wire: Current unbalance check	1	1	0.00000	0.00000	0.00000	0.00000
	2	2	29.08597	5.15204	29.58375	3.99014
	3	3	29.08596	-114.84788	29.58151	-116.00369
	4	4	29.08599	125.15210	29.58423	123.99474
	0	0	0.00000	0.00000	0.00000	0.00000
			0.00000	1.65097	-0.00163	-11.13656
R, X			r(m,1)	x(m,1)	r(m,1)	x(m,1)
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with r=1*10^-8 generally ok	1	1	0.52950	0.52950	0.52950	0.52950
	2	2	0.79350	0.79350	0.79350	0.79350
	3	3	0.79350	0.79350	0.79350	0.79350
	4	4	0.79350	0.79350	0.79350	0.79350
	0	0	0.00000	0.00000	0.00000	0.00000

Table 26: Test 1 Calculated powers, losses, minimum loss, power factor and apparent power during compensation

Calculate power components without compensation	MATLAB	RSCAD
	Ppoc(h) before opt reassgt	20152.53
Loss Is'h ^2 (h)	2013.89	2083.33
Pth(h) before comp	22166.42	22568.73
Totals		
Tot. Ppoc bef opt reassgt	20152.53	20485.40
Tot. loss Is' ^2 bef opt reass	2013.89	2083.33
Is'	44.88	45.64
Pth before comp	22166.42	22568.73
Calculate min. loss, PF and AP		
Vth'	493.96	494.66
I _A ' ^2 (min loss)	2013.69423	2081.18877
PF _{SYS} bef comp (by losses)	1.0000	0.9995
AP _{SYS} = Is' Vth'	22167.29	22578.18
Loss reduction poss.by comp.	0.194	2.138

Table 27 shows the DFT results applied to the injected compensating currents during compensation. In Simulink, the ideal controlled current source used for current injection is highly accurate except for the phase angles not exactly matching the reference value. In RSCAD, although the controller was stable, there was a maximum of 3 % steady-state error in the magnitude of the injected currents and 2 % steady-state error in their phase angles. These errors can be considered negligible for the purpose of demonstrating a proof of concept of the GPT method experimentally.

Table 27: Test 1 Fundamental frequency reference and injected compensating currents.

Phase	Ref rms	Ref angle	MATLAB		RSCAD	
			Injected rms	Injected angle	Injected rms	Injected angle
A	2.624	-84.232	2.624	-84.418	2.542	-85.979
B	2.624	155.767	2.624	155.582	2.544	-205.979
C	2.624	35.767	2.624	35.582	2.544	-325.977

4.1.4 Additional test 2 at DPSL

Figure 25 and Figure 26 show the PoC voltages and currents for 3-cycles before compensation in Simulink and RSCAD respectively. In Simulink, on each phase, the current was lagging the voltage by 31.788°. In RSCAD, the current was lagging the voltage by 32.689°. The difference is 2.76 % which can be considered negligible.

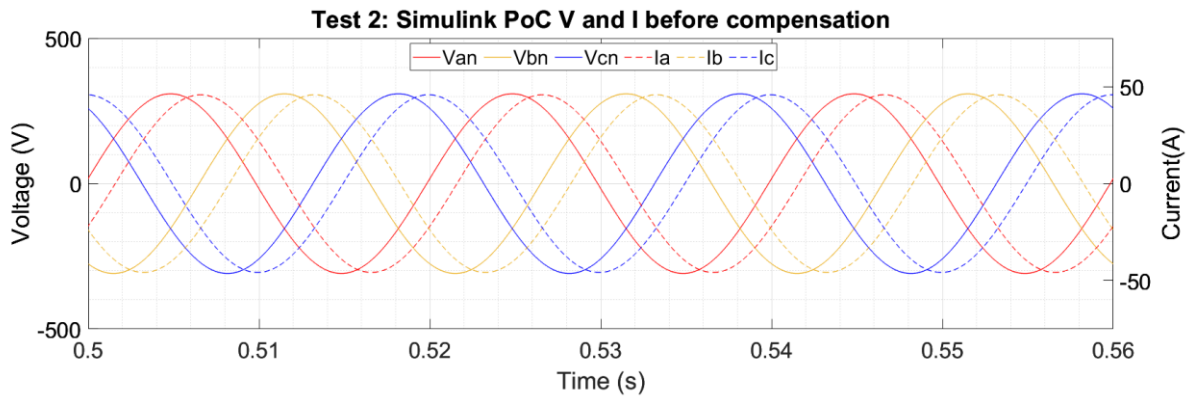


Figure 25: Test 2 Simulink results showing PoC V and I before compensation

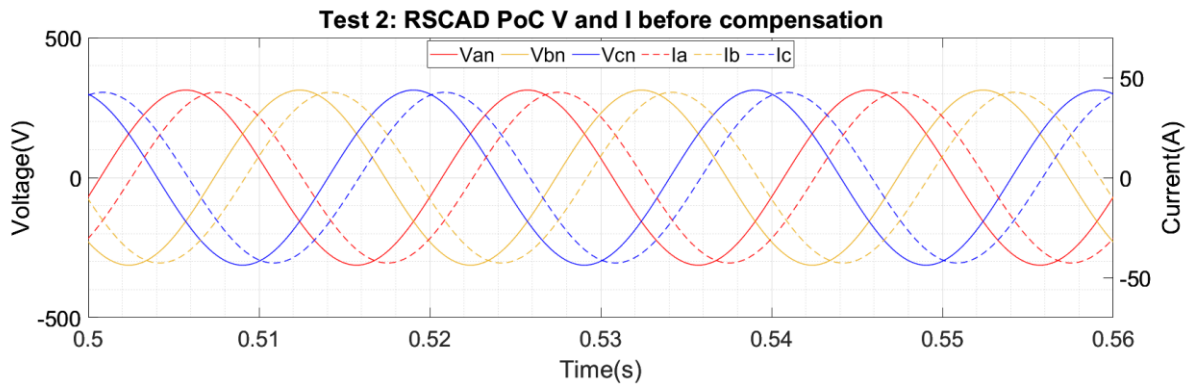


Figure 26: Test 2 RSCAD results showing PoC V and I before compensation

Table 28 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{AN} or V_{21} . The differences between MATLAB and RSCAD-based simulations are evident from the table. Although the exact same model of the network was developed in both software, they did not generate the same response.

Table 28: Test 2 Inputs to GPT Spreadsheet before compensation

INPUTS at PoC		m	Fund. freq h1			
			MATLAB		RSCAD	
CRMS voltages			$U_{m,h}$ [Vrms], α [deg]		$U_{m,h}$ [Vrms], α [deg]	
Voltage measure reference wire	1		0.00000	0.00000	0.00000	0.00000
	2		218.51356	0.00000	220.96447	0.00000
	3		218.51305	-119.99975	220.96459	-119.99993
	4		218.51414	120.00024	220.96450	120.00003
	0		0.00000	0.00000	0.00000	0.00000
CRMS currents			$I_{s,m,h}$ [A], α [deg]		$I_{s,m,h}$ [A], α [deg]	
If both U and $I=0$: insert $<1E-9$ to avoid Div0 condition in calcs Current unbalance calc below is useful for I in any last wire: Current unbalance check	1		0.00000	0.00000	0.00000	0.00000
	2		32.39784	-31.78806	30.17061	-32.68884
	3		32.39768	-151.78807	30.17060	-152.68881
	4		32.39776	88.21218	30.17061	87.31119
	0		0.00000	0.00000	0.00000	0.00000
	0		0.00000	49.37664	0.00000	153.72062
R, X			$r(m,1)$	$x(m,1)$	$r(m,1)$	$x(m,1)$
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with $r=1*10^{-8}$ generally ok	1		0.52950	0.52950	0.52950	0.52950
	2		0.79350	0.79350	0.79350	0.79350
	3		0.79350	0.79350	0.79350	0.79350
	4		0.79350	0.79350	0.79350	0.79350
	0		0.00000	0.00000	0.00000	0.00000

Table 29

Table 17: Test A1.2 Calculated powers, losses, minimum loss, power factor and apparent power before compensation

shows the power components calculated by the GPT. Differences in the measured PoC voltages and currents reflect, of course, in the power components. The powers delivered to the load at bus 3 in Simulink and RSCAD were 18.052 kW and 16.832 kW respectively. The Simulink system prior to compensation is apparently more efficient than the RSCAD test network as seen from the higher power factor in the former.

Table 29: Test 2 Calculated powers, losses, minimum loss, power factor and apparent power before compensation

Calculate power components without compensation		
	MATLAB	RSCAD
Ppoc(h) before opt reassgt	18052.38	16832.23
Loss $\ I_s'h\ ^2$ (h)	2498.61	2166.89
Pth(h) before comp	20550.99	18999.12
Totals		
Tot. Ppoc bef opt reassgt	18052.38	16832.23
Tot. loss $\ I_s'h\ ^2$ bef opt reass	2498.61	2166.89
$\ I_s'h\ $	49.99	46.55
Pth before comp	20550.99	18999.12
Calculate min. loss, PF and AP		
$\ V_{th}'\ $	493.96	494.16
$\ I_A'\ ^2$ (min loss)	1579.56212	1354.47026
PF _{sys} bef comp (by losses)	0.7951	0.7906
AP _{sys} = $\ I_s'h\ \ V_{th}'\ $	24691.30	23003.15
Loss reduction poss.by comp.	919.046	812.417

Table 30 shows the calculated and injected compensating currents in both MATLAB and RSCAD simulations. Although not exact, the compensating currents were closely matched including their angles with respect to their respective reference vector.

Table 30: Test 2 Calculated optimal compensating currents before compensation

Compensation approach: calculate currents		MATLAB		RSCAD	
$I_c(m,h)$:		I_c rms	I_c angle	I_c rms	I_c angle
1		0.00	43.15	0.00	-77.45
2		17.99853911	-84.28368488	17.04246	-84.78760
3		17.99854407	155.71608951	17.04247	155.21238
4		17.99848021	35.71618866	17.04246	35.21242
0		0.00	0.00	0.00	0.00
Check sum I_c		0.00		0.00	

Figure 27 and Figure 28 show the PoC voltages and currents for 3-cycles during compensation in Simulink and RSCAD respectively. The phase shift between currents and voltages was reduced in both software when compensation was introduced. The voltages and currents in the PHIL test bed are slightly distorted which shows that PHIL tests provide a more representative effect of compensation because it uses a physical power-electronic converter compared to an ideal controlled current source.

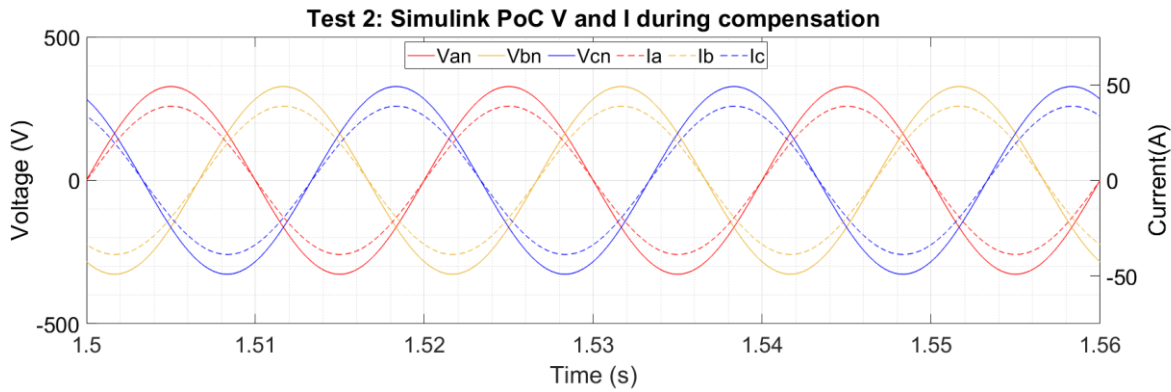


Figure 27: Test 2 Simulink results showing PoC V and I during compensation.

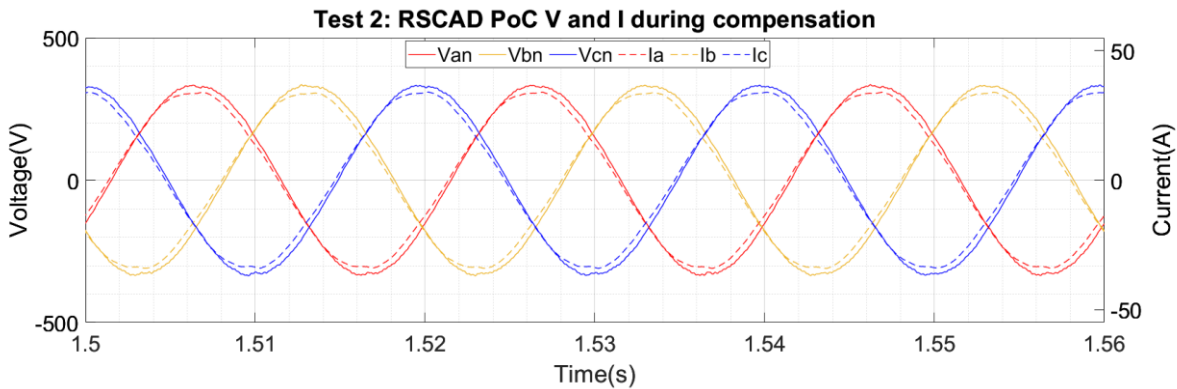


Figure 28: Test 2 RSCAD results showing PoC V and I during compensation.

Table 31 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{AN} or V_{21} . The differences between in MATLAB and RSCAD are evident from the table. In both cases, the voltage at the PoC increased upon injection of the compensating currents. Table 32 shows that the power factor of both the Simulink and RSCAD power system models was improved by GPT-compensation. The power consumed by the load increased in both software showing the effect of the constant impedance load to an increase in voltage.

Table 31: Test 2 Inputs to GPT Spreadsheet during compensation

INPUTS at PoC		m	Fund. freq h1			
CRMS voltages			MATLAB		RSCAD	
			Um,h [Vrms], α [deg]		Um,h [Vrms], α [deg]	
Voltage measure reference wire	1		0.00000	0.00000	0.00000	0.00000
	2		231.25104	0.00000	235.48620	0.00000
	3		231.23750	-119.98977	235.50844	-120.00803
	4		231.28003	120.00802	235.48967	119.99273
	0		0.00000	0.00000	0.00000	0.00000
CRMS currents			/s m,h [A], α [deg]		/s m,h [A], α [deg]	
If both U and I=0: insert $k < 1E-9$ to avoid Div0 condition in calcs Current unbalance calc below is useful for I in any last wire: Current unbalance check	1		0.00000	0.00000	0.00000	0.00000
	2		27.40711	-0.30769	24.11766	3.18364
	3		27.40552	-120.29746	24.12802	-116.76446
	4		27.41055	119.70031	24.13855	123.17562
	0		0.00000	0.00000	0.00000	0.00000
			0.00000	-8.14627	0.00000	0.00000
R, X			r(m,1)	x(m,1)	r(m,1)	x(m,1)
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with $r=1*10^{-8}$ generally ok	1		0.52950	0.52950	0.52950	0.52950
	2		0.79350	0.79350	0.79350	0.79350
	3		0.79350	0.79350	0.79350	0.79350
	4		0.79350	0.79350	0.79350	0.79350
	0		0.00000	0.00000	0.00000	0.00000

Table 32: Test 2 Calculate powers, losses, minimum loss, power factor and apparent power during compensation

Calculate power components without compensation		
	MATLAB	RSCAD
Ppoc(h) before opt reassgt	19014.35	17019.47
Loss $\ I_s^h\ ^2$ (h)	1788.19	1385.84
Pth(h) before comp	20802.54	18405.31
Totals		
Tot. Ppoc bef opt reassgt	19014.35	17019.47
Tot. loss $\ I_s^h\ ^2$ bef opt reass	1788.19	1385.84
$\ I_s\ $	42.29	37.23
Pth before comp	20802.54	18405.31
Calculate min. loss, PF and AP		
$\ V_{th}\ $	493.96	494.55
$\ I_A\ ^2$ (min loss)	1770.53895	1384.93765
PF _{sys} bef comp (by losses)	0.9951	0.9997
AP _{sys} = $\ I_s\ \ V_{th}\ $	20888.25	18410.42
Loss reduction poss.by comp.	17.653	0.904

Table 33 tabulates the reference and the injected compensating currents' rms and angle values in Simulink and RSCAD. With the ideal controlled current source in Simulink, negligible errors were found between the reference compensating currents and injected currents. In RSCAD, the converter injected currents with maximum steady-state errors of 2.5 %.

Table 33: Test 2 Reference and injected compensating currents.

Phase	Reference (MATLAB)		Reference (RSCAD)		
	rms	angle	rms	angle	
A	17.999	-84.284	17.04246	-84.78760	
B	17.999	155.716	17.04247	155.21238	
C	17.998	35.716	17.04246	35.21242	
Injected (MATLAB)		Injected (RSCAD)			
A	17.999	-84.451	16.61544	-89.01308	
B	17.999	155.537	16.64602	151.0120	
C	17.997	35.542	16.63207	30.92280	

4.1.5 Additional test A3 at DPSL

Figure 29 and Figure 30 show the PoC voltages and currents for 3-cycles before compensation in Simulink and RSCAD respectively. In both software, on each phase, the current was in phase with the voltage.

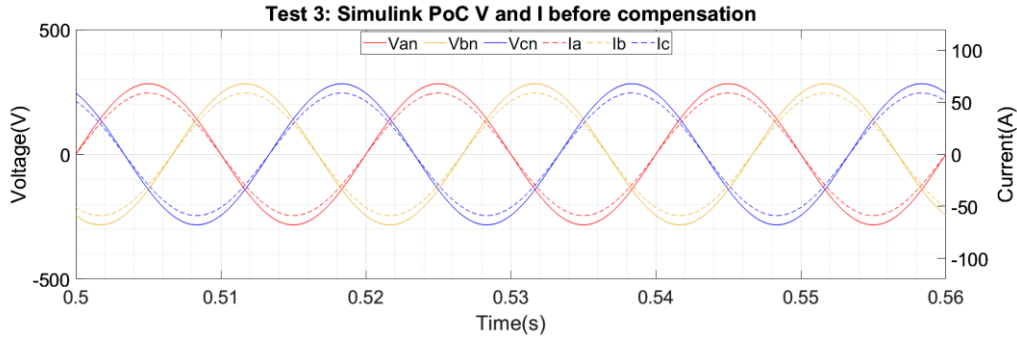


Figure 29: Test 3 Simulink results showing PoC V and I before compensation

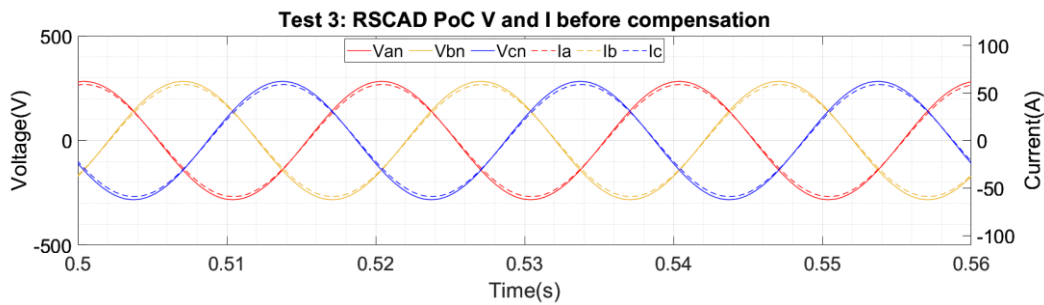


Figure 30: Test 3 RSCAD results showing PoC V and I before compensation

Table 34 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{AN} or V_{21} . The results before compensation matched very closely between Simulink and RSCAD.

Table 34: Test 3 Inputs to GPT Spreadsheet before compensation

INPUTS at PoC		m	Fund. freq h1			
			MATLAB		RSCAD	
CRMS voltages			$U_{m,h}$ [Vrms], α [deg]		$U_{m,h}$ [Vrms], α [deg]	
Voltage measure reference wire	1	1	0.00000	0.00000	0.00000	0.00000
	2	2	199.99981	0.00000	199.99538	0.00000
	3	3	199.99981	-120.00000	199.99539	-120.00000
	4	4	199.99981	120.00000	199.99539	-240.00000
	0	0	0.00000	0.00000	0.00000	0.00000
CRMS currents			$I_{s m,h}$ [A], α [deg]		$I_{s m,h}$ [A], α [deg]	
If both U and $I=0$: insert $<1E-9$ to avoid Div0 condition in calcs Current unbalance calc below is useful for I in any last wire: Current unbalance check	1	1	0.00000	0.00000	0.00000	0.00000
	2	2	41.66683	0.00000	41.66591	0.00000
	3	3	41.66683	-120.00000	41.66591	-120.00000
	4	4	41.66683	120.00000	41.66591	-240.00000
	0	0	0.00000	0.00000	0.00000	0.00000
			0.00000	0.75356	0.00000	167.35853
R, X			$r(m,1)$	$x(m,1)$	$r(m,1)$	$x(m,1)$
All r must be non-zero in delivery case, ignored in apparatus case.	1	1	0.48000	1.92000	0.48000	1.92000
	2	2	0.48000	1.92000	0.48000	1.92000
	3	3	0.48000	1.92000	0.48000	1.92000

Apparatus case approached with $r=1 \times 10^{-8}$ generally ok	4	0.48000	1.92000	0.48000	1.92000
	0	0.00000	0.00000	0.00000	0.00000

Table 35 shows the power components calculated by the GPT. Differences in the measured PoC voltages and currents reflect, of course, in the power components. The powers delivered to the load at bus 3 in Simulink and RSCAD were 25.000 kW and 24.998 kW respectively. The power factor before compensation was 0.9279. The GPT determines that it is possible to reduce the losses by 347 W by injecting compensating currents given in Table 36.

Table 35: Test 3 Calculated powers, losses, minimum loss, power factor and apparent power before compensation

Calculate power components without compensation		
	MATLAB	RSCAD
Ppoc(h) before opt reassgt	25000.07	24998.97
Loss $\ I_s'h\ ^2$ (h)	2500.02	2499.91
Pth(h) before comp	27500.09	27498.88
Totals		
Tot. Ppoc bef opt reassgt	25000.07	24998.97
Tot. loss $\ I_s'h\ ^2$ bef opt reass	2500.02	2499.91
$\ I_s'h\ $	50.00	50.00
Pth before comp	27500.09	27498.88
Calculate min. loss, PF and AP		
$\ V_{th}'\ $	585.23	585.22
$\ I_A'\ ^2$ (min loss)	2152.60740	2152.51214
PF _{sys} bef comp (by losses)	0.9279	0.9279
AP _{sys} = $\ I_s'h\ \ V_{th}'\ $	29261.86	29260.57
Loss reduction poss.by comp.	347.412	347.396

Table 36: Test 3 Calculated optimal compensating currents before compensation

Compensation approach: calculate currents I_c (m,h):		MATLAB		RSCAD	
		Ic rms	Ic angle	Ic rms	Ic angle
1		0.00	-11.45	0.000	134.99214
2		14.24799	-68.02710	14.24767	-68.02710
3		14.24799	171.97289	14.24767	171.97289
4		14.24799	51.97289	14.24767	51.97289
0		0.00	0.00	0.00000	0.00
Check sum I_c		0.00		0.00000	

Figure 31 and Figure 32 show the voltages and currents for 3-cycles during compensation in Simulink and RSCAD respectively. Compensation using the GPT introduced a phase shift between the PoC voltages and currents. This condition is identified by the GPT as the optimal operating condition with minimum delivery loss. The Simulink results are ideal in the sense that the controlled current source injects the compensating currents without introducing harmonic distortion (ThD = 0). On the other hand, RSCAD results revealed a distortion in the voltages (ThD < 0.68 %) and in the currents (ThD < 0.2 %) because the physical 10 kW converter introduces its own distortion during current injection.

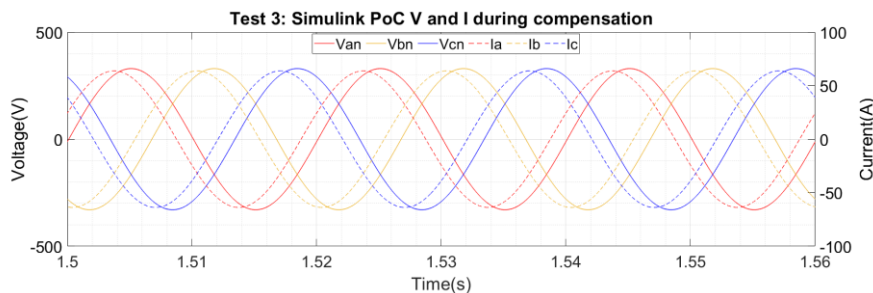


Figure 31: Test 3 Simulink results showing PoC V and I during compensation.

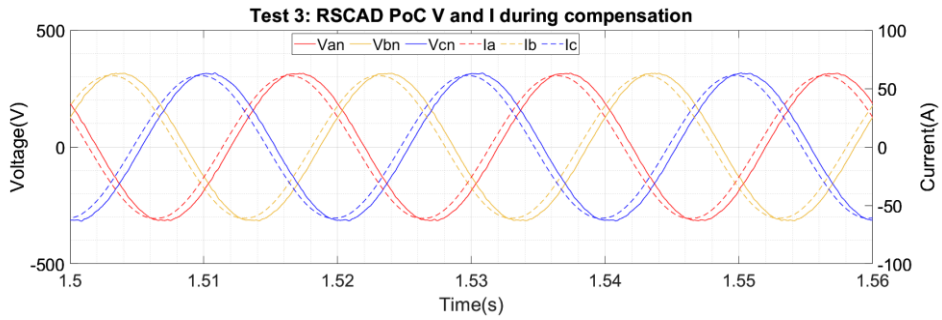


Figure 32: Test 3 RSCAD results showing PoC V and I during compensation.

Table 37 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{AN} or V_{21} . In both cases, the voltage at the PoC increased upon injection of the compensating currents. However, the increase in voltage was higher in Simulink than in RSCAD. The results further confirm the software differences when simulating the same model but with different methods of current injection.

Table 37: Test 3 Inputs to GPT Spreadsheet during compensation

INPUTS at PoC		m	Fund. freq h1			
CRMS voltages			MATLAB		RSCAD	
Voltage measure reference wire			$U_{m,h}$ [Vrms], α [deg]		$U_{m,h}$ [Vrms], α [deg]	
		1	0.00000	0.00000	0.00000	0.00000
		2	233.19084	0.00000	223.42083	0.00000
		3	233.19057	-120.00003	223.39110	-120.05112
		4	233.19060	120.00004	223.23336	119.98105
		0	0.00000	0.00000	0.00000	0.00000
CRMS currents			$I_{s m,h}$ [A], α [deg]		$I_{s m,h}$ [A], α [deg]	
If both U and $I=0$: insert $k<1E-9$ to avoid Div0 condition in calcs		1	0.00000	0.00000	0.00000	0.00000
Current unbalance calc below is useful for I in any last wire: Current unbalance check		2	45.10245	24.47898	43.31152	17.72882
		3	45.10208	-95.52120	43.41106	-102.29959
		4	45.10194	144.47885	43.34275	137.60065
		0	0.00000	0.00000	0.00000	0.00000
			-0.00040	24.45584	0.00000	-133.50460
R, X			$r(m,1)$	$x(m,1)$	$r(m,1)$	$x(m,1)$
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with $r=1*10^{-8}$ generally ok		1	0.48000	1.92000	0.48000	1.92000
		2	0.48000	1.92000	0.48000	1.92000
		3	0.48000	1.92000	0.48000	1.92000
		4	0.48000	1.92000	0.48000	1.92000
		0	0.00000	0.00000	0.00000	0.00000

Table 38 shows that the power factor of the Simulink and RSCAD power system models was improved by GPT-compensation. The power consumed by the load increased in both software showing the effect of the constant impedance load to an increase in voltage. Due to the constant impedance model of the load, both the Simulink-model and RSCAD model would need further (iterative) compensation to further reduce the delivery losses to a constant power load.

Table 38: Test 3 Calculate powers, losses, minimum loss, power factor and apparent power during compensation.

Calculate power components without compensation		
	MATLAB	RSCAD
Ppoc(h) before opt reassgt	28716.11	27674.69
Loss s'h ^2 (h)	2929.25	2706.72
Pth(h) before comp	31645.36	30381.41
Totals		
Tot. Ppoc bef opt reassgt	28716.11	27674.69
Tot. loss s' ^2 bef opt reass	2929.25	2706.72
s'	54.12	52.03
Pth before comp	31645.36	30381.41
Calculate min. loss, PF and AP		
Vth'	585.24	585.22
I _A ' ^2 (min loss)	2922.66031	2692.59189
PF _{SYS} bef comp (by losses)	0.9989	0.9974
AP _{SYS} = s' Vth'	31674.44	30446.86
Loss reduction poss.by comp.	6.594	14.129

Table 39 shows a comparison of the reference compensating currents and injected currents from the controlled current source in Simulink and the physical 10 kW converter. Negligible steady-state errors (< 0.3 %) were observed. Although not shown in this report, the compensating currents injected by the converter were distorted with harmonics. Odd harmonics (3rd, 5th and 7th) were the most dominant. The THD in the compensating currents was < 2.58 % on average for all 3-phases.

Table 39: Test 3 Reference and injected compensating currents

Phase	Reference (MATLAB)		Reference (RSCAD)	
	rms	angle	rms	angle
A	14.24799	-68.02710	14.24767	-68.02710
B	14.24799	171.97289	14.24767	171.97289
C	14.24799	51.97289	14.24767	51.97289
Phase	Injected (MATLAB)		Injected (RSCAD)	
	rms	angle	rms	angle
A	14.24797	-68.04551	14.21077	-68.13920
B	14.24789	171.95421	14.21884	171.38145
C	14.24787	51.95465	14.11169	51.59265

4.1.6 Additional test A4 at DPSL

Figure 33 and Figure 34 show the PoC voltages and currents for 3-cycles before compensation in Simulink and RSCAD respectively. In Simulink, on each phase, the current was lagging the voltage by 5.176°. In RSCAD, the current was lagging the voltage by 6.054°.

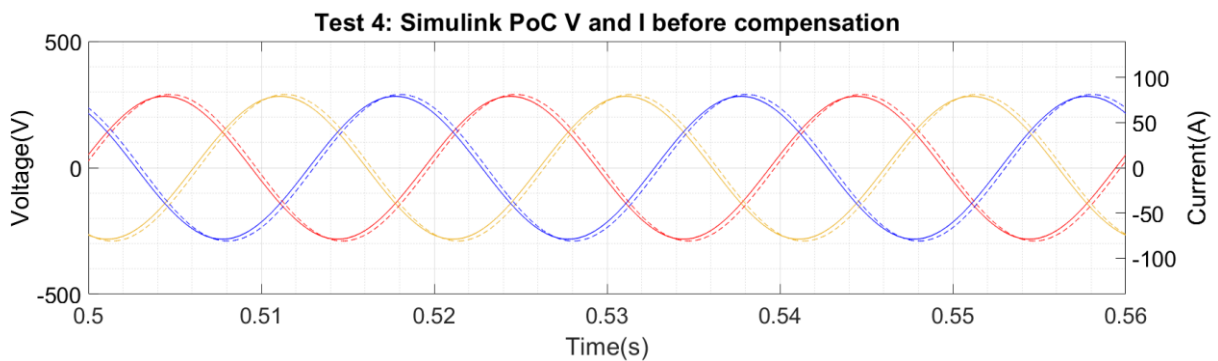


Figure 33: Test 4 Simulink results showing PoC V and I before compensation

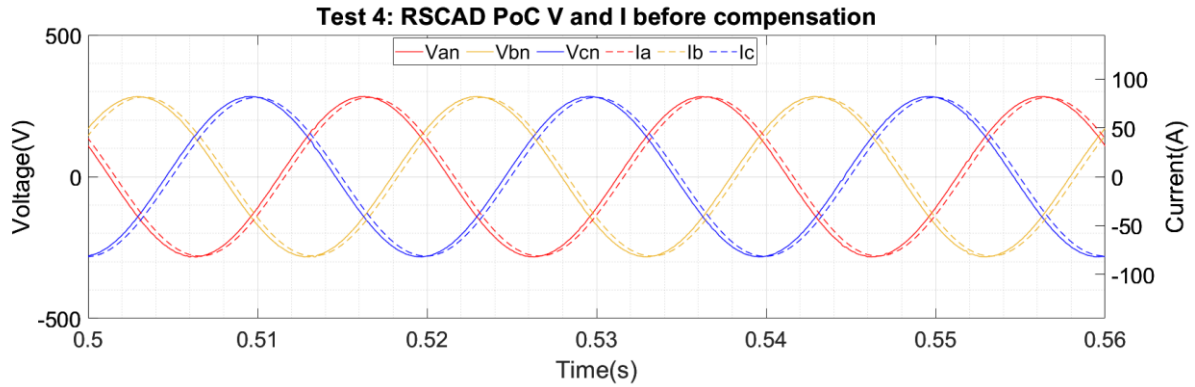


Figure 34: Test 4 RSCAD results showing PoC V and I before compensation

Table 40 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{AN} or V_{21} . The differences between in MATLAB and RSCAD are evident from the table.

Table 41 shows the power components calculated by the GPT. Differences in the measured PoC voltages and currents are reflected in the power components. The powers delivered to the load at bus 3 in Simulink and RSCAD were 34.230 kW and 34.183 kW respectively. The Simulink system prior to compensation is relatively more efficient than the RSCAD test network as seen from the higher power factor in the former.

Table 42 shows the calculated compensating currents in both MATLAB and RSCAD simulations. Although not exact, the compensating currents are closely matched including their angles with respect to their respective reference vector.

Table 40: Test 4 Inputs to GPT Spreadsheet before compensation

INPUTS at PoC		m	Fund. freq h1			
			MATLAB		RSCAD	
CRMS voltages			Um,h [Vrms], α [deg]		Um,h [Vrms], α [deg]	
Voltage measure reference wire	1	0.00000	0.00000	0.00000	0.00000	
	2	199.73584	0.00000	199.74594	0.00000	
	3	199.73584	-120.00000	199.74782	-120.00441	
	4	199.73584	120.00000	199.75213	-240.00328	
	0	0.00000	0.00000	0.00000	0.00000	
CRMS currents			/s m,h [A], α [deg]		/s m,h [A], α [deg]	
If both U and I=0: insert k<1E-9 to avoid Div0 condition in calcs Current unbalance calc below is useful for I in any last wire: Current unbalance check	1	0.00000	0.00000	0.00000	0.00000	
	2	57.35929	-5.17617	57.36006	-6.05427	
	3	57.35929	-125.17617	57.36293	-126.04950	
	4	57.35929	114.82383	57.36542	-246.05402	
	0	0.00000	0.00000	0.00000	0.00000	
R, X			r(m,1)	x(m,1)	r(m,1)	x(m,1)
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with r=1*10^-8 generally ok	1	0.48000	0.72000	0.48000	0.72000	
	2	0.48000	0.72000	0.48000	0.72000	
	3	0.48000	0.72000	0.48000	0.72000	
	4	0.48000	0.72000	0.48000	0.72000	
	0	0.00000	0.00000	0.00000	0.00000	

Table 41: Test 4 Calculated powers, losses, minimum loss, power factor and apparent power before compensation

Calculate power components without compensation		
	MATLAB	RSCAD
Ppoc(h) before opt reassgt	34229.96	34182.97
Loss $\ I_s'h\ ^2$ (h)	4737.73	4738.31
Pth(h) before comp	38967.68	38921.28
Totals		
Tot. Ppoc bef opt reassgt	34229.96	34182.97
Tot. loss $\ I_s'h\ ^2$ bef opt reass	4737.73	4738.31
$\ I_s'h\ $	68.83	68.84
Pth before comp	38967.68	38921.28
Calculate min. loss, PF and AP		
$\ V_{th}'\ $	585.23	586.52
$\ I_A'\ ^2$ (min loss)	4344.48999	4306.41062
PF _{sys} bef comp (by losses)	0.9576	0.9533
AP _{sys} = $\ I_s'h\ \ V_{th}'\ $	40282.39	40373.35
Loss reduction poss.by comp.	393.236	431.897

Table 42: Test 4 Calculated optimal compensating currents before compensation

Compensation approach: calculate currents $I_c(m,h)$:		MATLAB		RSCAD	
	1	lc rms	lc mag	lc rms	lc mag
	2	0.00	-37.62	0.0010680	113.5531488
	3	14.545402894	-78.291388872	15.2594887	-78.3453979
	4	14.545402953	161.708611022	15.2550845	161.6698249
	0	14.545402894	41.708610962	15.2600707	41.6723568
	0	0.00	0.00	0.0000000	0.00
	Check sum I_c	0.00		0.0004065	

Figure 35 and Figure 36 show the voltages and currents for 3-cycles during compensation in Simulink and RSCAD respectively. Before compensation, the currents were lagging the voltages in both software. During compensation, the currents lead the voltages by 8.841° in Simulink and 9.505° in RSCAD.

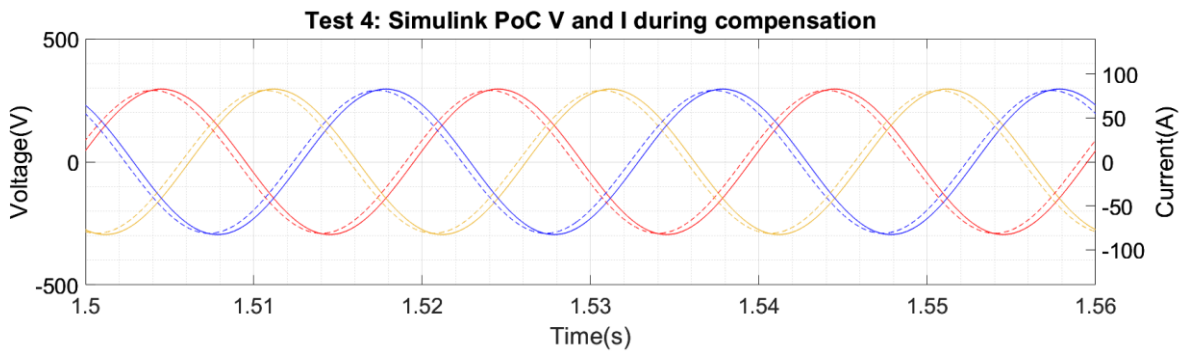


Figure 35: Test 4 Simulink results showing PoC V and I during compensation

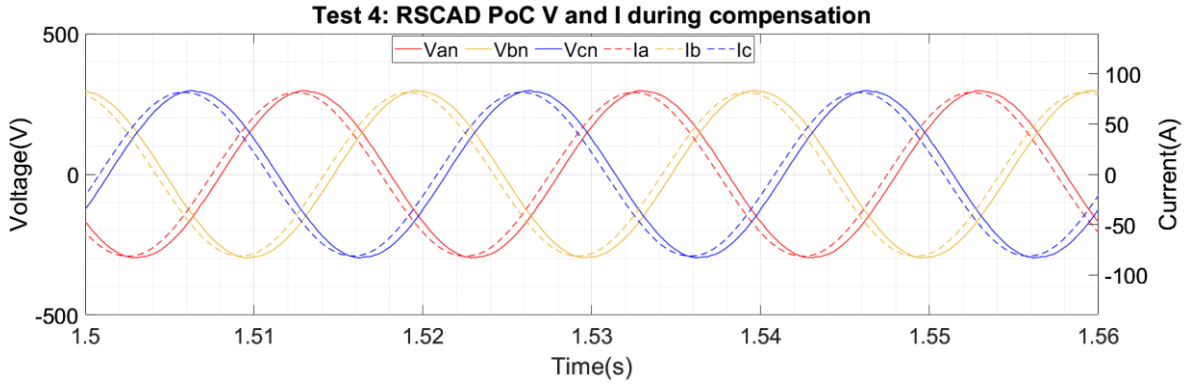


Figure 36: Test 4 RSCAD results showing PoC V and I during compensation.

Table 43 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{AN} or V_{21} . In both software, the voltage increased during compensation. The increase in voltage was higher in RSCAD as compared to MATLAB. Table 44 shows the power components during compensation. It can be observed that GPT compensation improved the efficiency of power delivery as seen from the higher power factor than before compensation. The load power increased since the constant impedance load draws due to the change in voltage.

Table 45 compares the reference compensating currents calculated from the simulation of the same model in MATLAB and RSCAD. In both software, the injected currents matched the reference with negligible steady-state errors.

Table 43: Test 4 Inputs to GPT Spreadsheet during compensation

INPUTS at PoC		m	Fund. freq h1			
			MATLAB		RSCAD	
CRMS voltages			$U_{m,h}$ [Vrms], α [deg]		$U_{m,h}$ [Vrms], α [deg]	
Voltage measure reference wire	1	0.00000	0.00000	0.00000	0.00000	0.00000
	2	208.81300	0.00000	209.68651	0.00000	
	3	208.81708	-120.00034	209.67183	-119.99837	
	4	208.81395	119.99886	209.69315	120.00289	
	0	0.00000	0.00000	0.00000	0.00000	0.00000
CRMS currents			I_s m,h [A], α [deg]		I_s m,h [A], α [deg]	
If both U and $I=0$: insert $<1E-9$ to avoid Div0 condition in calcs Current unbalance calc below is useful for I in any last wire: Current unbalance check	1	0.00000	0.00000	0.00000	0.00000	0.00000
	2	57.45388	8.84050	57.70441	9.50543	
	3	57.45322	-111.15462	57.69755	-110.51491	
	4	57.45778	128.84351	57.68531	129.49912	
	0	0.00000	0.00000	0.00000	0.00000	0.00000
R, X			$r(m,1)$	$x(m,1)$	$r(m,1)$	$x(m,1)$
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with $r=1*10^{-8}$ generally ok	1	0.48000	0.72000	0.48000	0.72000	0.72000
	2	0.48000	0.72000	0.48000	0.72000	0.72000
	3	0.48000	0.72000	0.48000	0.72000	0.72000
	4	0.48000	0.72000	0.48000	0.72000	0.72000
	0	0.00000	0.00000	0.00000	0.00000	0.00000

Table 44: Test 4 Calculated powers, losses, minimum loss, power factor and apparent power during compensation

Calculate power components without compensation		
	MATLAB	RSCAD
Ppoc(h) before opt reassgt	35564.43	35796.38
Loss $\ I_s^h\ ^2$ (h)	4753.54	4793.47
Pth(h) before comp	40317.97	40589.85
Totals		
Tot. Ppoc bef opt reassgt	35564.43	35796.38
Tot. loss $\ I_s^h\ ^2$ bef opt reass	4753.54	4793.47
$\ I_s^h\ $	68.95	69.23
Pth before comp	40317.97	40589.85
Calculate min. loss, PF and AP		
$\ V_{th}\ $	585.23	586.52
$\ I_A\ ^2$ (min loss)	4743.80662	4787.96503
PF _{sys} bef comp (by losses)	0.9990	0.9994
AP _{sys} = $\ I_s^h\ \ V_{th}\ $	40349.59	40607.68
Loss reduction poss.by comp.	9.738	5.508

Table 45: Test 4 Reference and injected compensating currents

Phase	Reference (MATLAB)		Reference (RSCAD)	
	rms	angle	rms	angle
A	14.54540	-78.29139	15.25949	-78.34540
B	14.54540	161.70861	15.25508	161.66982
C	14.54540	41.70861	15.26007	41.67236
Phase	Injected (MATLAB)		Injected (RSCAD)	
	rms	angle	rms	angle
A	14.54216	-78.29603	15.27154	-78.44517
B	14.54775	161.70960	15.24845	161.57005
C	14.54618	41.68768	15.26352	41.63748

4.1.7 Additional test A5 at DPSL

Figure 37 and Figure 38 show the PoC voltages and currents for 3-cycles before compensation in Simulink and RSCAD respectively. In Simulink, on each phase, the current was lagging the voltage by 31.788°. In RSCAD, the current was lagging the voltage by 32.689°. The difference is 2.76 % which can be considered negligible.

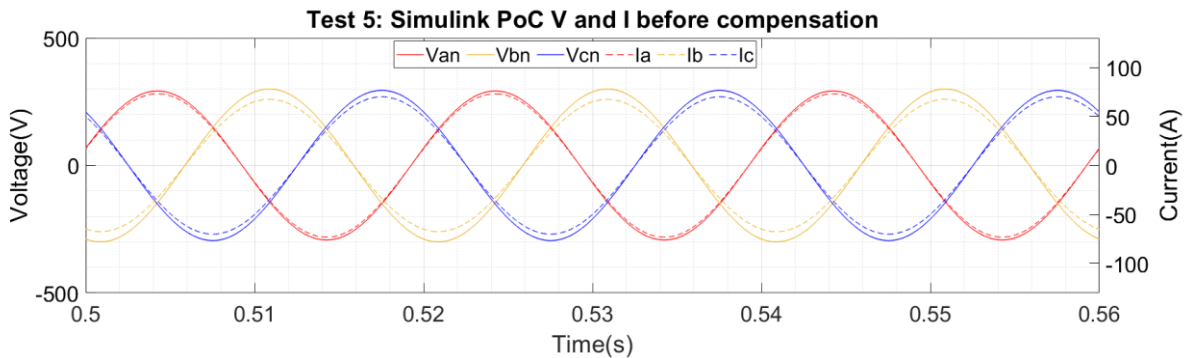


Figure 37: Test 5 Simulink results showing PoC V and I before compensation

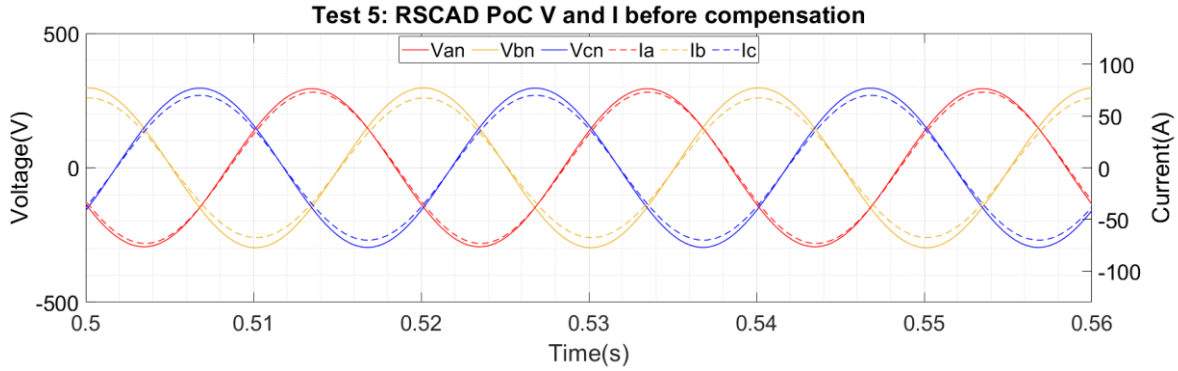


Figure 38: Test 5 RSCAD results showing PoC V and I before compensation

Table 46 shows the CRMS values of PoC voltages and currents, and their angles with respect to a common reference phasor chosen as V_{AN} or V_{21} . The differences between in MATLAB and RSCAD are evident from the table. Table 47 shows the power components calculated by the GPT. Differences in the measured PoC voltages and currents reflect, of course, in the power components. The powers delivered to the load at bus 3 in Simulink and RSCAD were 18.052 kW and 16.832 kW respectively. The Simulink system prior to compensation is apparently more efficient than the RSCAD test network as seen from the higher power factor in the former.

Table 46: Test 5 Inputs to GPT Spreadsheet before compensation

INPUTS at PoC		m	Fund. freq h1			
			MATLAB		RSCAD	
CRMS voltages			$U_{m,h}$ [Vrms], α [deg]		$U_{m,h}$ [Vrms], α [deg]	
Voltage measure reference wire	1	0.00000	0.00000	0.00000	0.00000	
	2	206.72932	0.00000	207.78647	0.00000	
	3	212.06589	-119.13058	210.05955	240.42029	
	4	208.38214	121.11904	209.31256	120.15874	
	0	0.00000	0.00000	0.00000	0.00000	
CRMS currents			$I_{s m,h}$ [A], α [deg]		$I_{s m,h}$ [A], α [deg]	
If both U and $I=0$: insert $k<1E-9$ to avoid Div0 condition in calcs	1	2.95839	-166.52627	2.95837	-167.89917	
	2	51.68254	0.00000	51.68234	-1.37203	
	3	47.71504	-119.13058	47.71491	239.49739	
Current unbalance calc below is useful for I in any last wire: Current unbalance check	4	49.49097	121.11904	49.49076	119.74699	
	0	0.00000	0.00000	0.00000	0.00000	
	0	0.00000	27.67475	0.00000	180.00000	
R, X			$r(m,1)$	$x(m,1)$	$r(m,1)$	$x(m,1)$
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with $r=1*10^{-8}$ generally ok	1	0.48000	0.48000	0.48000	0.48000	
	2	0.48000	0.48000	0.48000	0.48000	
	3	0.48000	0.48000	0.48000	0.48000	
	4	0.48000	0.48000	0.48000	0.48000	
	0	0.00000	0.00000	0.00000	0.00000	

Table 47: Test 5 Calculated powers, losses, minimum loss, power factor and apparent power before compensation

Calculate power components without compensation		
	MATLAB	RSCAD
Ppoc(h) before opt reassgt	31116.06	31116.26
Loss $\ I_s'h\ ^2$ (h)	3554.84	3554.81
Pth(h) before comp	34670.90	34671.07
Totals		
Tot. Ppoc bef opt reassgt	31116.06	31116.26
Tot. loss $\ I_s'h\ ^2$ bef opt reass	3554.84	3554.81

$\ I_s'\ $	59.62	59.62
Pth before comp	34670.90	34671.07
Calculate min. loss, PF and AP		
$\ V_{th}'\ $	585.23	586.07
$\ I_A'\ ^2$ (min loss)	3498.24951	3485.84922
PF _{sys} bef comp (by losses)	0.9920	0.9903
AP _{sys} = $\ I_s'\ \ V_{th}'\ $	34893.16	34942.72
Loss reduction poss.by comp.	56.591	68.966

Table 48 shows the calculated compensating currents in both MATLAB and RSCAD simulations. Although not exact, the compensating currents are closely matched including their angles with respect to their respective reference vector.

Table 48: Test 5 Calculated optimal compensating currents before compensation

Compensation approach: calculate currents $I_c(m,h)$:		MATLAB		RSCAD	
		lc rms	lc mag	lc rms	lc mag
1		2.96	-166.53	2.7426930	-
2		6.20720	-64.09815	6.9421966	-67.3594543
3		5.02070	135.44795	5.6219835	138.5510864
4		4.64524	36.30924	5.2351547	35.5176357
0		0.00	0.00	0.0000000	0.00
	Check sum I_c	0.00		0.0000000	

Figure 39 and Figure 40 show the PoC voltages and currents for 3-cycles during compensation in Simulink and RSCAD respectively. The phase shift between currents and voltages was reduced in both Simulink and RSCAD. The voltages and currents in the PHIL test bed are slightly distorted which shows that PHIL tests provide a more representative effect of compensation using a power-electronic converter compared to a controlled current source.

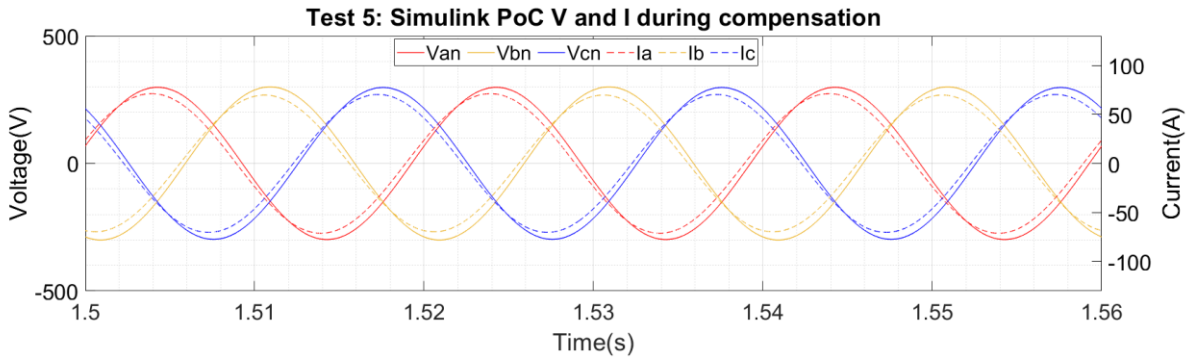


Figure 39: Test 5 Simulink results showing PoC V and I during compensation

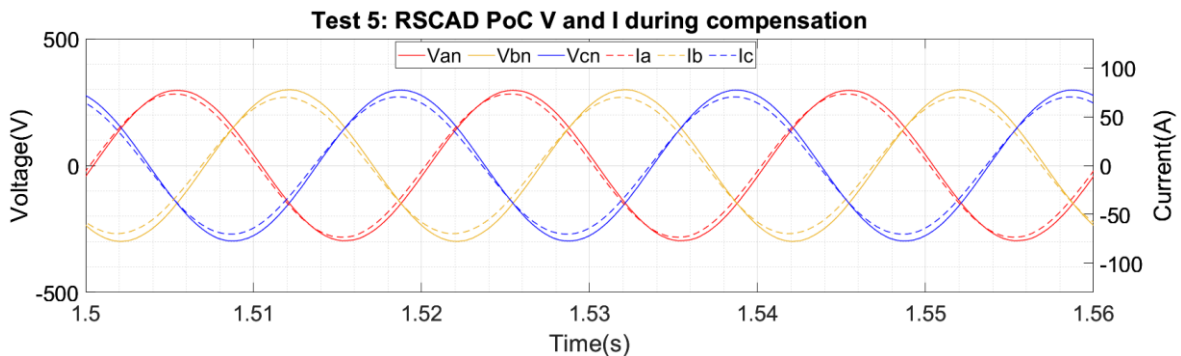


Figure 40: Test 5 RSCAD results showing PoC V and I during compensation

Table 49 shows the CRMS values of PoC voltages and currents, and their angles with respect

to a common reference phasor chosen as V_{AN} or V_{21} . The differences between in MATLAB and RSCAD are evident from the table. In both cases, the voltage at the PoC increased upon injection of the compensating currents. The introduction of the compensating currents reduced the voltage and current imbalance in the network.

Table 49: Test 5 Inputs to GPT Spreadsheet during compensation

INPUTS at PoC		m	Fund. freq h1			
			MATLAB		RSCAD	
CRMS voltages			Um,h [Vrms], α [deg]		Um,h [Vrms], α [deg]	
Voltage measure reference wire	1	0.00000	0.00000	0.00000	0.00000	
	2	211.04137	0.00000	209.76457	0.00000	
	3	212.27768	-119.50586	210.96689	-119.66529	
	4	210.47669	120.51078	210.49061	120.37186	
	0	0.00000	0.00000	0.00000	0.00000	
CRMS currents			/s m,h [A], α [deg]		/s m,h [A], α [deg]	
If both U and I=0: insert $k < 1E-9$ to avoid Div0 condition in calcs Current unbalance calc below is useful for I in any last wire: Current unbalance check	1	1.26445	-141.13911	2.97663	-168.08491	
	2	50.32717	6.35262	51.94089	3.85909	
	3	49.27900	-113.85101	49.41929	-115.93324	
	4	49.70856	125.84224	49.72507	123.29752	
	0	0.00000	0.00000	0.00000	0.00000	
	0	0.00000	126.92360	0.00000	0	
R, X			r(m,1)	x(m,1)	r(m,1)	x(m,1)
All r must be non-zero in delivery case, ignored in apparatus case. Apparatus case approached with $r=1 \cdot 10^{-8}$ generally ok	1	0.48000	0.48000	0.48000	0.48000	
	2	0.48000	0.48000	0.48000	0.48000	
	3	0.48000	0.48000	0.48000	0.48000	
	4	0.48000	0.48000	0.48000	0.48000	
	0	0.00000	0.00000	0.00000	0.00000	

Table 50 shows that the power factor of the Simulink and RSCAD power system models was improved by GPT-compensation. The power consumed by the load increased in both software showing the effect of the constant impedance load to an increase in voltage. The Simulink-model would need further compensation to further reduce the delivery losses. Instead, the RSCAD power system model has already been optimised and becomes more efficient in delivering power when compensation is introduced.

Table 50: Test 5 Calculated powers, losses, minimum loss, power factor and apparent power during compensation

Calculate power components without compensation		
	MATLAB	RSCAD
Ppoc(h) before opt reassgt	31383.05	31727.40
Loss Is'h ² (h)	3568.22	3658.35
Pth(h) before comp	34951.27	35385.75
Totals		
Tot. Ppoc bef opt reassgt	31383.05	31727.40
Tot. loss Is' ² bef opt reass	3568.22	3658.35
Is'	59.73	60.48
Pth before comp	34951.27	35385.75
Calculate min. loss, PF and AP		
Vth'	585.23	586.15
I _A ' ² (min loss)	3566.29825	3640.89200
PF _{sys} bef comp (by losses)	0.9997	0.9976
AP _{sys} = Is' Vth'	34958.75	35452.99
Loss reduction poss.by comp.	1.918	17.459

Table 51 tabulates the reference and the injected compensating currents' rms and angle in Simulink and RSCAD. With the controlled current source, negligible errors were found between the reference compensating currents and injected currents. In RSCAD, the converter injected

currents with small steady-state errors of around 2.5 %.

Table 51: Test 5 Reference and injected compensating currents

Phase	Reference (MATLAB)		Reference (RSCAD)	
	rms	angle	rms	angle
A	6.20720	-64.09815	6.94219	-67.35945
B	5.02070	135.44795	5.62198	138.55108
C	4.64524	36.30924	5.23515	35.51763
Injected (MATLAB)		Injected (RSCAD)		
A	6.20713	-63.78243	6.72519	-84.14921
B	5.02077	135.76294	5.97795	4.22705
C	4.64520	36.62424	4.09537	132.8152

4.1.8 Test C1 at PNDC

Post-processing of the measurement data from different meters is discussed in detail in Appendix A. Post-processing the PNDC measurements. Since the measurements from different meters started at different times, they had to be synchronised in time before the results could be analysed. Time synchronisation of the Fluke and Beckhoff Data Acquisition Systems during different time intervals identified for analysis is discussed in Appendix B. Time-synchronisation of Fluke and . Correction factors applied to each Fluke meter to synchronise it to the Beckhoff Data Acquisition System are given in Appendix B. Time-synchronisation of Fluke and . The MATLAB script developed to handle post-processing and time synchronisation is shown in Appendix C. MATLAB script for post-processing and time synchronisation

To calculate the power, a Simulink model was developed which imports post-processed measurement data from the Fluke and Beckhoff Data Acquisition System. Currents I_A , I_B , I_C were imported. With regards to the voltages, only V_{AB} , and V_{CA} were imported. In a three-wire system with phase A as the reference, only two voltage measurements are required to analyse the system performance.

An FFT is then carried out on the voltages and currents. Then, from the magnitudes, the CRMS values of V and I are calculated and from the angles, the phase angles of V and I can be identified. The angular reference was taken from vector V_{BA} measured for Beckhoff D1.

4-time intervals were identified for analysis as shown in Table 75 in Appendix B. Tables 52 to 55 show the CRMS values of voltages and currents measured in time intervals t_1 to t_4 . Harmonic voltage and current components were negligible compared to the fundamental frequency components. Hence, FFT results are shown for fundamental frequency only.

Table 52: Test C1 t_1 CRMS values of V and I at each bus before compensation t_1 (B: Beckhoff; F: Fluke).

Bus	V_{BA}	V_{CA}	I_A	I_B	I_C
1	428.12 \angle 34.91	428.18 \angle -25.37	64.24 \angle 192.92	64.95 \angle 73.33	65.00 \angle -47.41
2	426.87 \angle 37.25	426.98 \angle -23.04	64.21 \angle 195.30	64.70 \angle 75.71	64.85 \angle -44.87
3 (B)	418.14 \angle 0.00	420.19 \angle -60.22	65.96 \angle 194.52	64.50 \angle 74.86	65.59 \angle -44.20
3 (F)	No measurement data before compensation				

Table 53: Test C1 h1 CRMS values of V and I at each bus before compensation t2 (B: Beckhoff; F: Fluke).

Bus	V _{BA}	V _{CA}	I _A	I _B	I _C
1	428.57∠-323.41	429.61∠-23.58	86.25∠206.39	85.72∠-273.30	86.39∠-33.15
2	429.00∠-323.53	427.73∠-23.44	86.61∠206.41	85.30∠-273.48	86.10∠-32.79
3 (B)	418.05∠0.00	420.68∠-60.05	88.01∠206.71	85.18∠-272.87	87.18∠-31.47
3 (F)	419.26∠0.36	421.34∠-59.98	35.57∠31.18	34.54∠-86.89	36.09∠-206.45

Table 54: Test C1 h1 CRMS values of V and I at each bus before compensation t3 (B: Beckhoff; F: Fluke).

Bus	V _{BA}	V _{CA}	I _A	I _B	I _C
1	428.01∠37.68	428.87∠337.30	86.29∠207.28	85.70∠87.66	86.49∠327.81
2	426.95∠35.91	428.87∠335.83	86.49∠205.62	85.19∠86.20	86.60∠326.66
3 (B)	417.06∠0.00	421.05∠299.89	87.93∠206.58	85.09∠87.11	87.23∠328.45
3 (F)	418.77∠-0.35	420.34∠298.95	35.69∠29.87	34.37∠272.04	36.19∠152.74

Table 55: Test C1 h1 CRMS values of V and I at each bus before compensation t4 (B: Beckhoff; F: Fluke).

Bus	V _{BA}	V _{CA}	I _A	I _B	I _C
1	427.15∠34.72	427.54∠334.36	62.96∠184.21	63.92∠64.57	63.79∠303.65
2	427.33∠32.92	426.60∠332.88	63.18∠182.64	63.73∠62.68	63.50∠302.23
3 (B)	416.62∠0.00	419.69∠299.80	64.67∠185.59	63.30∠66.13	64.52∠306.91
3 (F)	418.59∠361.29	419.85∠300.81	0.04∠322.11	0.04∠246.29	0.06∠102.27

Using the measurements from Tables 52 and 55, the fundamental frequency power was calculated at each bus during time intervals t1 to t4. The results are shown in Table 56. The power losses along each feeder are shown in Table 57. The power loss in feeder 2-3 was significantly high. We suspect that the uncalibrated Beckhoff Data Acquisition System may have captured “bad data” which did not truly represent the PoC measurements.

Table 56: Test C1 Fundamental frequency power at each bus at different time intervals

Bus	P _{T1} (W)	P _{T2} (W)	P _{T3} (W)	P _{T4} (W)
1	47582.77	60159.57	60173	47125.21
2	47332.37	59840.40	59898.33	46946.85
3 (B)	33531.30	33986.26	34052.24	37541.97
3 (F)	No data	-11979.72	-12042.25	-31.53

Table 57: Test C1 Fundamental frequency power loss in each branch at different time intervals

Line	P _{T1} (W)	P _{T2} (W)	P _{T3} (W)	P _{T5} (W)
1-2	250.40	319.17	274.69	178.36
2-3	13801.07	25854.15	25846.09	9404.88

Using the currents measured in each feeder and the power losses calculated from Table 57, the cable resistance was calculated during time intervals t1 to t4. An example calculation for time interval t1 is shown. The calculated cable resistances during different time intervals are given in Table 58, showing also the values from the two previous tables for easy inspection of the differences.

Cable resistance calculation during time interval t1

Power loss in branch 1-2 before compensation = 250.40 W

$$(I_a^2 + I_b^2 + I_c^2)R = 250.40 \text{ W}$$

$$R = \frac{250.40}{(I_a^2 + I_b^2 + I_c^2)} = \frac{250.40}{(64.24^2 + 64.95^2 + 65.00^2)}$$

Resistance of cables = $R = 0.0199186 \Omega$

Cable length between bus 1 and 2 = 115 m

Resistance per meter = 0.000173205 $\Omega/100\text{m}$

Power loss in branch 2-3 with compensation = 13801.07 W

$$(I_a^2 + I_b^2 + I_c^2)R = 13801.07 \text{ W}$$

$$\text{Assumed balanced resistances } R = \frac{13801.07}{(I_a^2 + I_b^2 + I_c^2)} = \frac{13801.07}{(64.24^2 + 64.95^2 + 65.00^2)}$$

Resistance of cables = $R = 1.0979127 \Omega$

Cable length between bus 2 and 3 = 455 m

Resistance per meter = 0.241299 $\Omega/100\text{m}$

Table 58: Test C1 Fundamental frequency power measurements and derived resistances R1-2 and R2-3 in Ohms per 100 m in each branch at different time intervals

Bus or Branch	At t1 (before comp.)	At t2 (with comp.)	At t3 (with comp.)	At t4 (after comp.)
P ₁ [W]	47582.77	60159.57	60173	47125.21
P ₂ [W]	47332.37	59840.40	59898.33	46946.85
P ₃ [W]	33531.30	33986.26	34052.24	37541.97
LossP ₁₋₂ [W]	250.40	319.17	274.69	178.36
LossP ₂₋₃ [W]	13801.07	25854.15	25846.09	9404.88
R ₁₋₂ [Ω/100m]	0.0173205	0.0124729	0.0107249	0.0127990
R ₂₋₃ [Ω/100m]	0.241299	0.255379	0.255057	0.17058

We expected the value of the resistance of each branch to be the same during time intervals t3 and t5 and the resistance/100 m of both branches to be the same. However, the apparent cable resistance was neither the same for a branch under both loading conditions (before, with and after compensation) nor for the two branches under the same loading. The nature of the apparent changes in unit resistance are inconsistent. A small variation due to temperature is expected but this is not the case here, after analysing different time intervals and both branches. Notwithstanding the comment following Table 55 about the uncalibrated Backhoff meter at Bus 3, the variation in resistance/100 m is derived from two calibrated Fluke meters of the same type, and they also indicate inconsistent derived resistances.

Based on the observation that the currents and power increased with compensation, instead of decreasing as expected, an investigation of the compensating currents was made, described below.

Figure 41 shows the measured compensator output currents and the controller’s current reference when synchronised to the voltage reference phasor V_{BA}. To generate the current reference, the measured line to line voltage V_{AB} at bus D1 from the Fluke meter was converted to V_{BA} using V_{BA} = -V_{AB}. The voltage V_{BA} was used as input to the PLL. Therefore, if the PLL locks to V_{BA}, Figure 41 reveals that there is a 150-degree phase shift between the measured output current and the current reference for each phase. The 150-degree phase shift implies that the currents injected by the compensator were incorrect since they do not match the reference currents.

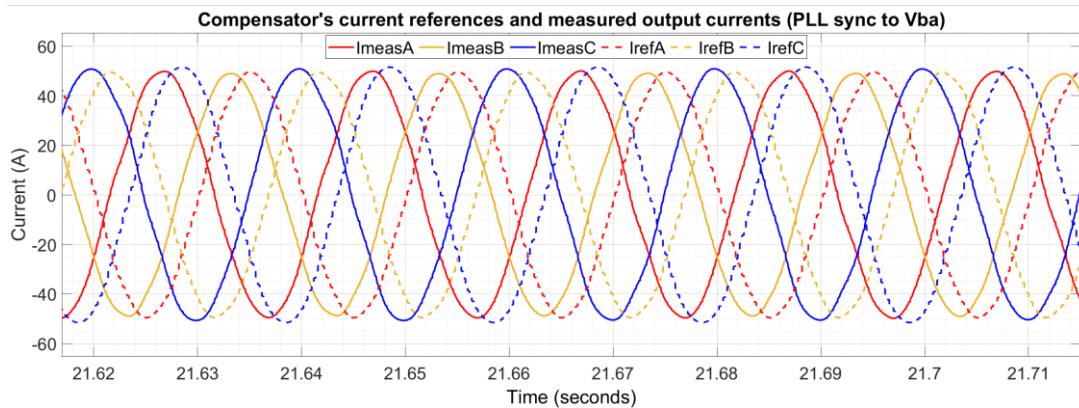


Figure 41: Test C1 Measured compensator output (solid lines) currents and controller’s current

references (dotted lines) generated from the PLL locked to phasor V_{BA}

Figure 42 shows the measured compensator output currents and the controller's current reference when synchronised to the V_{AN} where N is a virtual neutral on the measurement PCB of the converter. In this case, to compare the measured currents and references, the PLL was synchronised to V_{AN} which was generated using the measured line to line voltages V_{AB} , phase shifted by 30 degrees (leading). The phase shift was added because V_{AN} leads V_{AB} by 30-degrees. When the current references are synchronised to V_{AN} , there is a relatively small phase shift between the references and measured compensator outputs.

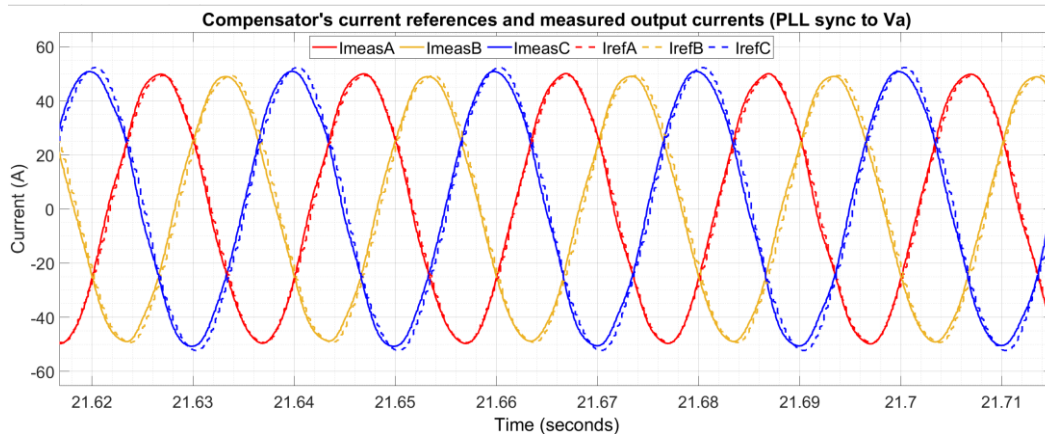


Figure 42: Test C1 Measured compensator output (solid lines) currents and controller's current references (dot-ted lines) generated from the PLL locked to phasor V_{AN}

The results show that the converter PLL did not synchronise to the voltage vector V_{BA} but instead locked to the vector V_{AN} . In the controller, a setting (0 or 1) changes the input to the PLL from being either V_{BA} or V_{AN} . This setting was wrongly adjusted to use V_{AN} as the input to the PLL.

Even though the calculated compensating currents were not synchronised to the correct reference voltage, measurement of the power at each end of branch 1-2, and inconsistency of the derived resistance, still shows that problems are evident in the physical test circuit or the measurement system.

4.1.9 Test C2 at PNDC

Post-processing of test C2 measurement data from different meters is discussed in detail in Appendix A. Post-processing the PNDC measurements. Since the measurements from different meters started at different times, they had to be synchronised in time before the results could be analysed. Time synchronisation of the Fluke and Beckhoff Data Acquisition Systems during different time intervals identified for analysis in test C2 is discussed in Appendix B. Time-synchronisation of Fluke and . Correction factors applied to each Fluke meter to synchronise it to the Beckhoff Data Acquisition System are given in Appendix B. Time-synchronisation of Fluke and .

To calculate the power, the same Simulink model as used for analysing results from test C1 was used. 4-time intervals were identified for analysis as shown in Table B2.5 in Appendix B. Tables 59 to 62 show the CRMS values of voltages and currents measured in time intervals t1 to t4. Harmonic voltage and current components were negligible compared to the fundamental frequency components. Hence, FFT results are shown for fundamental frequency only.

Table 59: Test C2 h1 CRMS values of V and I at each bus before compensation t1 (B: Beckhoff; F: Fluke).

Bus	V _{BA}	V _{CA}	I _A	I _B	I _C
1	422.49∠35.69	425.14∠-24.57	105.60∠-193.77	95.33∠22.72	63.66∠-76.71
2	420.17∠35.71	423.29∠-24.67	105.41∠-193.87	94.99∠22.62	63.52∠-76.66
3 (B)	406.53∠0.00	416.39∠-59.92	107.11∠-193.39	94.84∠23.11	64.32∠-74.70
3 (F)	No measurement data from Fluke D1 before compensation				

Table 60: Test C2 h1 CRMS values of V and I at each bus before compensation t2 (B: Beckhoff; F: Fluke).

Bus	V _{BA}	V _{CA}	I _A	I _B	I _C
1	420.89∠36.53	426.94∠336.10	125.24∠-183.71	104.76∠15.31	43.03∠303.80
2	418.19∠36.55	425.26∠335.90	124.92∠-183.79	104.46∠15.22	42.93∠303.76
3 (B)	404.43∠0.00	422.32∠300.60	126.23∠-183.48	104.32∠15.56	43.82∠305.59
3 (F)	403.16∠0.75	416.81∠298.90	28.18∠-0.31	17.99∠107.82	28.32∠216.81

Table 61: Test C2 h1 CRMS values of V and I at each bus before compensation t3 (B: Beckhoff; F: Fluke).

Bus	V _{BA}	V _{CA}	I _A	I _B	I _C
1	421.51∠37.48	428.00∠337.38	125.73∠-182.55	105.84∠15.93	42.05∠304.52
2	418.80∠37.20	426.42∠336.92	125.48∠-182.93	105.53∠15.52	41.94∠304.29
3 (B)	404.95∠0.00	421.36∠300.47	126.41∠-183.43	105.12∠15.13	42.84∠305.23
3 (F)	404.66∠2.08	416.44∠300.39	28.37∠-359.18	19.11∠109.65	28.64∠219.99

Table 62: Test C2 h1 CRMS values of V and I at each bus before compensation t4 (B: Beckhoff; F: Fluke).

Bus	V _{BA}	V _{CA}	I _A	I _B	I _C
1	422.91∠36.04	425.58∠-24.13	105.77∠-193.47	95.49∠22.95	63.65∠-76.44
2	420.72∠35.03	423.94∠-25.24	105.58∠-194.59	95.20∠21.82	63.50∠-77.44
3 (B)	406.90∠0.00	416.57∠-59.85	107.10∠-193.43	95.01∠23.05	64.29∠-75.91
3 (F)	407.93∠0.38	413.85∠-60.66	0.03∠-70.23	0.04∠-100.62	0.07∠91.40

Using the measurements from Tables 59 to 62, the fundamental frequency power was calculated at each bus during time intervals t1 to t4. The results are shown in Table 63. The power losses along each feeder are shown in Table 64. The power measured at bus 3 was higher than the power at bus 2. As in test C1, the Beckhoff measurements at bus 3 appeared to be giving inconsistent results.

Table 63: Test C2 Fundamental frequency power at each bus at different time intervals

Bus	P _{T1} (W)	P _{T2} (W)	P _{T3} (W)	P _{T4} (W)
1	55860.60	56631.21	56611.72	55898.31
2	55434.33	56149.31	56131.28	55491.96
3 (B)	61356.43	59080.15	59079.22	61438.98
3 (F)	No data	-504.01	-347.70	-28.15

Table 64: Test C2 Fundamental frequency power loss in each branch at different time intervals

Line	P _{T1} (W)	P _{T2} (W)	P _{T3} (W)	P _{T4} (W)
1-2	426.27	481.9	480.44	406.35
2-3	-5922.1	-2930.84	-2947.94	-5947.02

Table 65 shows the calculated powers, losses and derived cable resistances in feeders 1-2 and 2-3 from test C2 measurement data. Since the power loss along feeder 2-3 was negative, the cable resistance in feeder 2-3 was calculated assuming power flows from bus 3 to bus 2.

The trend of reducing magnitude of R_{1-2} is contrary to the effect that would be caused by temperature rise in the cables during the few minutes of the test. There are some instances where the cable resistance during different time intervals were matched. However, the “varying resistance” phenomenon interpreted from the measurement data does not represent true power system characteristics.

Table 65: Test C2 Fundamental frequency power measurements and derived resistances R_{1-2} and R_{2-3} in Ohms per 100 m in each branch at different time intervals

Bus or Branch	At t1 (before comp.)	At t2 (with comp.)	At t3 (with comp.)	At t4 (after comp.)
P ₁ [W]	55860.60	56631.21	56611.72	55898.31
P ₂ [W]	55434.33	56149.31	56131.28	55491.96
P ₃ [W]	61356.43	59080.15	59079.22	61438.98
LossP ₁₋₂ [W]	426.27	481.9	480.44	406.35
R ₁₋₂ [Ω/100m]	0.0152591	0.0146980	0.0145173	0.0145073
R ₂₋₃ [Ω/100m]	0.0538515	0.0227143	0.0226214	0.0539133

To further analyse the results, a last study was conducted using test C2 measurement data within the defined time intervals for analysis. The frequency of the measured currents during different time intervals was calculated during 5 cycles described as follows:

- One cycle prior to the sampled 3-cycle time interval.
- First cycle of sampled 3-cycle time interval.
- Second cycle of sampled 3-cycle time interval.
- Third cycle of sampled 3-cycle time interval.
- One cycle after the sampled 3-cycle time interval.

Table 66 shows the frequencies calculated for each cycle during time intervals t1 to t4 using measurement data from Fluke F2 at bus 1. The same process was repeated for measurements from Fluke F1 at bus 2 and the frequencies are shown in Table 67. The results showed that, even after synchronisation of the Fluke meters, the signals could not be perfectly aligned since the measurement data is exported with a variable sampling frequency. Data points around the zero-crossing may be missed or offset although the interpolation technique applied to post-process the measurement data was effective in producing meaningful waveforms for analysis.

Table 66: Test C2 – Frequency of each current cycles and adjacent cycles in A-phase at Bus 1 during each time interval. Note measurements at bus 1 were made using Fluke meter F2.

	t1	t2	t3	t4
Prior cycle	49.986534627	50.000399353	50.005635635	50.017036428
1st cycle of sample	49.974394619	50.015171852	50.019347984	50.018549454
2nd cycle of sample	49.988327725	50.004161596	50.016578495	50.016006598
3rd cycle of sample	49.980218829	50.003102192	50.015632636	50.012214996
Following cycle	50.100731619	49.999373833	50.017094843	50.026447119

Table 67: Test C2 – Frequency of each current cycles and adjacent cycles in A-phase at Bus 2 during each time interval. Note measurements at bus 2 were made using Fluke meter F1.

	t1	t2	t3	t4
Prior cycle	49.98967713	49.99205126	50.02276036	50.00350025
1st cycle of sample	49.97356398	50.01277826	50.02926712	50.04629282
2nd cycle of sample	49.97174098	50.02966759	50.00575066	50.01275325
3rd cycle of sample	50.01740606	50.00670090	49.98600392	49.98400512
Following cycle	49.97993306	49.97661095	49.98925231	49.99875003

4.1.10 Tests C5, C6 at PNDC

There was insufficient time to fully implement tests C5 and C6 that required operation of the regenerative controllable load at Bus 2. We observed negligible harmonic distortion at the PoC despite the reduction in load in the final test protocol. However, in setting up for the tests, it became evident that the settings of positive and negative harmonic current inputs could establish combinations not representative of physical loads, which raises questions about the interpretation of results from real-laboratory testing when a regenerative controllable load is used.

4.1.11 Repeat of synchronisation after correcting phase voltage measurements to line voltage measurements

After going through a first attempt to synchronise the measurements at PNDC, since analysis of the results showed that the values of the cable resistance were inconsistent, a discussion exposed the possibility of a problem related to the Beckhoff DAQ. This was subsequently confirmed by PNDC as being that the DAQ measured virtual phase voltages and not line voltages as interpreted. Therefore, a second synchronisation of the test C1 data measurement

data was required, which is presented below.

An FFT is then carried out on the voltages and currents. Then, from the magnitudes, the CRMS values of V and I are calculated and, from the angles, the phase angle of V and I can be identified. The angular reference was taken from vector V_{BA} measured for Beckhoff D1.

Table 68: **h1** CRMS values of V and I at each bus **before compensation t1** (B – Beckhoff and F – Fluke).

Bus	V_{BA}	V_{CA}	I_A	I_B	I_C
1	426.919∠4.15 3	427.703∠303.80 0	62.897∠153.81 9	63.858∠34.23 5	63.781∠273.28 1
2	426.731∠5.69 8	426.831∠305.60 7	63.195∠155.55 9	63.654∠35.69 7	63.558∠275.27 1
3 (B)	416.640∠0.00 0	417.493∠299.50 9	64.712∠155.74 2	63.470∠36.04 4	64.392∠276.84 9
3 (F)	No measurement data from Fluke D1 before compensation				

Table 69: **h1** CRMS values of V and I at each bus **during compensation t2** (B – Beckhoff and F – Fluke).

Bus	V_{BA}	V_{CA}	I_A	I_B	I_C
1	428.575∠6.37 4	429.612∠306.20 0	86.070∠175.97 3	85.369∠56.48 9	86.389∠296.63 3
2	429.002∠6.25 2	427.731∠306.34 2	86.610∠176.19 0	85.301∠56.29 8	86.104∠296.99 8
3 (B)	417.662∠0.00 0	419.266∠299.65 5	86.174∠176.53 1	85.648∠57.50 9	87.179∠297.31 8
3 (F)	419.250∠1.77 9	421.345∠301.42 4	35.261∠32.386	34.532∠274.5 08	36.083∠154.96 4

Table 70: **h1** CRMS values of V and I at each bus **during compensation t3** (B – Beckhoff and F – Fluke).

Bus	V_{BA}	V_{CA}	I_A	I_B	I_C
1	428.011∠7.35 3	428.866∠306.97 5	86.073∠176.78 7	85.373∠57.38 0	86.493∠297.484
2	426.949∠5.58 1	428.866∠305.50 5	86.488∠175.29 7	85.187∠55.88 0	86.600∠296.331
3 (B)	416.927∠0.00 0	418.831∠299.46 6	87.931∠176.25 5	85.091∠56.78 3	87.235∠298.130
3 (F)	418.615∠- 1.026	420.685∠298.40 4	35.617∠29.209	34.368∠271.5 25	36.226∠152.057

Table 71: **h1** CRMS values of V and I at each bus **after compensation t4** (B – Beckhoff and F – Fluke).

Bus	V _{BA}	V _{CA}	I _A	I _B	I _C
1	427.139∠4.470	427.525∠-55.891	62.955∠153.96 3	63.919∠34.32 4	63.789∠-86.605
2	427.316∠2.674	426.593∠-57.376	63.179∠152.38 5	63.727∠32.43 6	63.504∠-88.018
3 (B)	416.873∠0.000	417.723∠-60.476	64.667∠155.33 8	63.303∠35.88 1	64.520∠-83.344
3 (F)	418.690∠0.258	419.748∠-60.244	0.032∠-49.179	0.041∠-114.511	0.065∠-259.900

Table 72: Fundamental frequency power at each bus and different time intervals

Bus	P _{T1} (W)	P _{T2} (W)	P _{T3} (W)	P _{T4} (W)
1	47090.30	60058.53	60060.52	47125.18
2	46937.98	59840.40	59897.98	46946.91
3 (B)	46189.77	55736.53	55961.84	46214.66
3 (F)	No data	-11982.66	-12045.37	-32.78

Table 73: Fundamental frequency power loss in each branch at different time intervals

Line	P _{T1} (W)	P _{T2} (W)	P _{T3} (W)	P _{T4} (W)
1-2	152.32	218.13	162.54	178.27
2-3	748.21	4103.87	3936.14	732.25

Table 74 summarises the power at each bus, the loss in each feeder and the calculated resistance between buses 1-2 and 2-3.

Table 74: Test C1 Fundamental frequency power measurements and derived resistances R1-2 and R2-3 in Ohms per 100 m in each branch at different time intervals

Bus or Branch	At t1 (before comp.)	At t2 (with comp.)	At t3 (with comp.)	At t4 (after comp.)
P ₁ [W]	47090.30	60058.53	60060.52	47125.18
P ₂ [W]	46937.98	59840.40	59897.98	46946.91
P ₃ [W]	46189.77	55736.53	55961.84	46214.66
LossP ₁₋₂ [W]	152.32	218.13	162.54	178.27
LossP ₂₋₃ [W]	748.21	4103.87	3936.14	732.25
R ₁₋₂ [Ω/100m]	0.0109450	0.0085600	0.0063729	0.0127921
R ₂₋₃ [Ω/100m]	0.0136069	0.0406441	0.0389036	0.0133165

The results from Table 74 show that even after resynchronisation, the values of the branch resistance were still not constant. This reality check still identifies that the test network or the measurement systems may have been setup incorrectly after the replacement of the faulty cable as discussed in section 3.1.3.

4.2 Conclusions

Analysis of the PHIL results showed the following:

1. For test A1.1, the voltage and current data measured from the RTDS were not captured long enough after the system had settled post-compensation in the first attempt to the PHIL tests. Measurement data from the 10 kW converter showed that after the system settled post-compensation, the reference compensating currents matched the injected currents from the converter. However, this post-compensation steady-state time interval was not captured in the RTDS data.
2. For test A1.2, the results have shown that the GPT compensates for the avoidable loss when supplying a balanced resistive and inductive load without the need to use reactive power as a concept.
3. The results of the additional five PHIL tests (including test A1.1 mentioned in (1) above) carried out at DPSL have shown that compensation for balanced resistive load, balanced resistive and inductive load, and an unbalanced resistive and inductive load is possible using the GPT.
4. PHIL simulation results are highly dependent on the models of power system components available in software.
5. The stability of the PHIL test bed is an important factor that must be accounted for when testing the response of power-electronic converter controllers.

Analysis of the results collected at PNDC showed the following:

1. There is unknown and potentially significant (non-negligible) uncertainty associated with the sampling times of data downloaded from the Fluke instruments. Unlike instruments from Yokogawa and SIRIUS Dewesoft, sampling is not at fixed intervals and the Fluke time stamps of measurement samples are not revealed consistently and with adequate resolution for the tests in these experiments. This limitation of the measurement system became evident only during the testing.
2. The Beckhoff Data Acquisition System was known to be uncalibrated and was used only to capture data at a fixed and high sampling rate to supplement the three available Fluke meters. The measurements derived from it have been shown to be unreliable, at least for the timer, but possibly also for other parameters that lead to values of power at Bus 3 that are unlikely to be valid. With hindsight, it might have been acceptable to use this meter only to measure the inverter output and use the third Fluke meter in the main feeder for its consistency with the meters at Bus 1 and Bus 2.
3. Even after careful attempts to perfectly time-synchronise measurements from the meters, the power measured at Bus 3, and consequently the power loss in feeder 2-3 was physically unlikely and significantly uncertain.
4. Calculation of the cable resistance in each of the branches 1-2 and 2-3 of the feeder showed that the values were inconsistent, without clear association according to the current magnitude, arising from changing frequency, or being with or without compensation. This is an unusual and unexpected finding and inconsistent with the physics of circuits.

5. The Beckhoff DAQ system was set to measure phase voltages with respect to a virtual neutral instead of measuring line voltages as required for the tests. This meant that all the measurements used to calculate the reference converter currents were incorrect.
6. There is non-negligible uncertainty that the Fluke and Beckhoff Data Acquisition Systems were giving consistent voltage and current data. There is some measurement error that introduces uncertainty.
7. Although the testing with the regenerative controllable load was not completed, some combinations of the settings of such equipment to emulate a physical load like a rectifier might not represent accurately the practical physical performance.
8. A good experience was gained at PNDC that will lead to successful tests in the future.

The challenges faced during experimental testing at PNDC, solutions and lessons learnt during the process have been discussed in a paper presented at the eGrid 2023 conference [19].

5 Open Issues and Suggestions for Improvements

Before making suggestions for improvement, it is important to record that the staff of the DPSL and PNDC were very helpful, as were several other interested persons in the research centre at the University of Strathclyde, and the comments here are not in any way of criticism of them or the efforts they made. The decision to allow the retrofitting of a novel control system to the Host's converter in the DPSL is just one example of the outstanding collaboration by the Host Institution.

Several factors, including the delayed signing of the contract, contributed to the late delivery of the test inverter from South Africa. However, the most critical one turned out to be a lack of communication about the information needed to avoid delays in customs documentation compliance, which delayed the equipment coming into the UK.

The Host Institution is very familiar with qualification or compliance tests on apparatus. However, it is less familiar with this project's unusual need to test the effects of an apparatus on the power system. (Such focus is evident also in the ERIGrid test description templates.) The User Group was unaware of many of the limitations of the laboratories until very late in the planning of the experiments. Issues faced with data collection as mentioned in the report might have been avoided by a preliminary visit for careful inspection and interrogation of the laboratories which would likely have made the experimentation much more productive at the expense of significant travel costs. In our opinion, the nature of the experiments would not have been appreciated better or been easier to carry out at any other laboratory in the ERIGrid consortium.

In terms of open issues, the User Group came to understand in a new way that both PHIL and real-laboratory testing can be set up in ways (or with models) that are not fully representative of real physical power system performance. This does not appear to be widely understood.

References

- [1] Malengret, M., & Gaunt, C.T. (2008). Decomposition of currents in three- and four-wire systems. *IEEE Trans on Instr. and Measurement*, vol 57, Issue 5, pp 963-972, <https://doi.org/10.1109/TIM.2007.911705>.
- [2] Malengret, M., & Gaunt, C.T. (2011). General theory of instantaneous power for multi-phase systems with distortion, unbalance and direct current components. *Electr. Power Syst. Res.*, vol. 81, pp 1897-1904, <https://doi.org/10.1016/j.epsr.2011.05.016>.
- [3] Malengret, M., & Gaunt, C.T. (2012). General theory of average power for multi-phase systems with distortion, unbalance and direct current components. *Electr. Power Syst. Res.*, vol. 84, pp. 224-230, <https://doi.org/10.1016/j.epsr.2011.11.020>.
- [4] Gaunt, C.T., & Malengret, M. (2012). True power factor metering for m-wire power systems with distortion, unbalance and direct current components. *Electr. Power Syst. Res.*, vol. 95, pp. 140-147, <https://doi.org/10.1016/j.epsr.2012.07.019>.
- [5] Simoes, M.G., Harirchi, F., & Babakmehr, M. (2019). Survey on time-domain power theories and their applications for renewable energy integration in smart-grids. *IET Smart Grid*, vol. 2, issue 4, p.491–503, <https://doi.org/10.1049/iet-stg.2018.0244>.
- [6] Frequency domain-based determination of currents for injection into a power network, UK patent GB2582914, B, 29 September 2021.
- [7] Malengret, M., & Gaunt, C.T. (2020). Active currents, power factor, and apparent power for practical power delivery systems. *IEEE Access*, <https://doi.org/10.1109/ACCESS.2020.3010638>.
- [8] NEMA (2011). Definitions for Calculations of VA, VAh, VAR, and VARh for Poly-Phase Electricity Meters. NEMA C12.24 TR-2011, National Electrical Manufacturers Association, Rosslyn, VA, USA, 2011.
- [9] Berrisford, A.J. (2012). Smart meters should be smarter. *IEEE Power and Energy Society General Meeting*, San Diego, USA, <https://doi.org/10.1109/PESGM.2012.6345146>.
- [10] Ndungu, C. Private communications, Sep 2020 – Dec 2021.
- [11] Malengret, M., & Gaunt, C.T. (2016). Inverters and compensators for minimum line losses. *Conf. on Power Electron. and Appl. and Exhibition (EPE)*, Karlsruhe, Germany, <https://doi.org/10.1109/EPE.2016.7695634>.
- [12] El-Habrouk, M., Darwish, M.K., & Mehta, P. (2000). A survey of active filters and reactive power compensation techniques. *Eighth International Conference on Power Electronics and Variable Speed Drives*, no. 475, pp. 18–19, <https://doi.org/10.1049/cp:20000211>.
- [13] Mariun, N., Alam, A., Mahmud, S. & H. Hizam, (2004). Review of control strategies for power quality conditioners. *Natl. Power Energy Conf. PECon 2004 - Proc.*, pp. 109–115, <https://doi.org/10.1109/pecon.2004.1461626>.
- [14] Lin, X., Gao, S., Li, J., Lei, H., & Kang, Y. (2011). A new control strategy to balance neutral-point voltage in three-level NPC inverter. *8th Int. Conf. Power Electron. ECCE Asia*, pp. 2593–2597, <https://doi.org/10.1109/ICPE.2011.5944742>.
- [15] Jankee, P., Oyedokun, D.T.O., & Chisepo, H.K. (2022). Network unbalance compensation comparison: conventional pq theory vs the general power theory. *IEEE PES/IAS*

PowerAfrica, Kigali, Rwanda, <https://doi.org/10.1109/PowerAfrica53997.2022.9905291>.

[16] Chisepo, H.K., & Gaunt, C.T., (2022). Towards asymmetrical modeling of voltage stability in the presence of GICs. IEEE PES/IAS PowerAfrica, Kigali, Rwanda, <https://doi.org/10.1109/PowerAfrica53997.2022.9905396>.

[17] Chisepo, H.K., Gaunt, C.T., & Jankee, P. (2022). Applying and comparing the general power theory compensation for unbalance and harmonics. Universities Power Engineering Conf., Istanbul, Turkey, <https://doi.org/10.1109/UPEC55022.2022.9917879>.

[18] Chisepo, H.K., & Gaunt, C.T. (2023). Network analysis and compensation of underground cable capacitive effects. South African Universities Power Engineering Conf., Johannesburg, <https://doi.org/10.1109/SAUPEC57889.2023.10057823>.

[19] Jankee, P, Gaunt, C. T., Malengret, M, Adbulhadi, I, Feizifar, B, Feng, Z, Burt, G. (2023). Challenges, Solutions and Lessons Learnt from Testing Power System Performance with a General Power Theory-Controlled Converter. 8th IEEE Workshop on the Electronic Grid., Karlsruhe, Germany – in press

Appendix A. Post-processing the PNDC measurements

A.1. Post-processing measurement data from Fluke meter

Measurement data from the Fluke meters can only be exported as a .txt file delimited using a tab. Moreover, the sampling rate of the data in “Waveform Capture” mode is unknown to the user. The data analysis revealed that there are random occurrences of the same timestamp, and multiple values of the measured quantity are associated with each timestamp. An example is shown in Figure 43.

Date	Time	AB(V)	BC(V)	CA(V)	A(A)	B(A)	C(A)			
2023/05/04	11:00:07.947				-282.428	595.456	-312.985	42.992	-43.449	0.076
2023/05/04	11:00:07.947				-320.451	595.499	-275.005	45.052	-40.703	-4.654
2023/05/04	11:00:07.948				-360.804	591.917	-231.070	46.425	-37.689	-9.041
2023/05/04	11:00:07.948				-400.467	585.702	-185.193	47.684	-35.515	-12.512
2023/05/04	11:00:07.948				-438.705	578.581	-139.876	49.477	-33.264	-16.518
2023/05/04	11:00:07.948				-474.181	567.964	-93.783	50.392	-29.259	-21.400
2023/05/04	11:00:07.949				-503.917	548.888	-44.928	50.545	-23.956	-26.855
2023/05/04	11:00:07.949				-527.741	521.526	6.172	50.392	-18.883	-31.815
2023/05/04	11:00:07.949				-546.083	487.776	58.307	49.858	-15.450	-34.676
2023/05/04	11:00:07.949				-560.843	451.782	109.061	49.515	-13.008	-36.697
2023/05/04	11:00:07.950				-572.712	413.673	159.039	48.676	-9.689	-39.177
2023/05/04	11:00:07.950				-580.912	372.932	207.937	47.112	-5.684	-41.580
2023/05/04	11:00:07.950				-584.925	334.477	250.405	45.815	-2.213	-43.678
2023/05/04	11:00:07.950				-586.781	291.794	294.944	44.022	2.022	-46.158
2023/05/04	11:00:07.951				-586.436	249.585	336.851	41.389	6.638	-48.065
2023/05/04	11:00:07.951				-582.293	204.700	377.593	38.452	10.567	-49.019
2023/05/04	11:00:07.951				-575.690	158.780	416.910	36.087	13.924	-50.011
2023/05/04	11:00:07.952				-567.360	113.377	453.940	33.264	18.501	-51.651
2023/05/04	11:00:07.952				-554.110	65.730	488.380	28.915	23.537	-52.376
2023/05/04	11:00:07.952				-531.797	14.890	516.865	23.689	27.962	-51.498
2023/05/04	11:00:07.952				-502.018	-36.124	538.142	19.417	31.929	-51.193
2023/05/04	11:00:07.953				-468.009	-88.345	556.398	16.174	34.866	-50.850
2023/05/04	11:00:07.953				-430.677	-140.222	570.942	13.046	36.697	-49.477
2023/05/04	11:00:07.953				-391.101	-188.602	579.703	9.613	39.063	-48.447
2023/05/04	11:00:07.953				-350.101	-236.206	586.307	5.836	41.809	-47.417

Figure 43: Sample .txt file produced using the export function from the Fluke meters. The data processing revealed irregular instances where a single timestamp appears multiple times, and each timestamp is associated with multiple values of the measured quantity.

To overcome this issue, a MATLAB script was developed that:

1. Reads data in the .txt files from all Fluke meters and generates a separate variable for the measurement timestamp, voltages, and currents.
2. Converts the measurement timestamps into a time axis in seconds.
3. Finds data points representing identical times in seconds and generates a new time axis with no repeated time data.
4. For each set of identical time points, finds the corresponding set of voltage or current measurements and calculate the average of the voltage or current.
5. Replaces the original measured voltages and currents with their average values calculated in step 4.
6. Upscales the data to 5 kHz sampling frequency.
7. Generates a timeseries with the upscaled data to represent each measured quantity.

Figure 44 shows an example of the results obtained after post-processing the exported data from one of the Fluke meters. The original exported data distorts the waveform since there

multiple values of the measured quantity are associated with each timestamp. The post-processed data is much more efficient for analysing the voltages and currents as it produces a smooth waveform. Unfortunately, one of the limitations of the post-processing approach is the approximation of the measured quantity (average voltages or currents for identical timestamps) resulting in harmonic distortion in the voltages or currents.

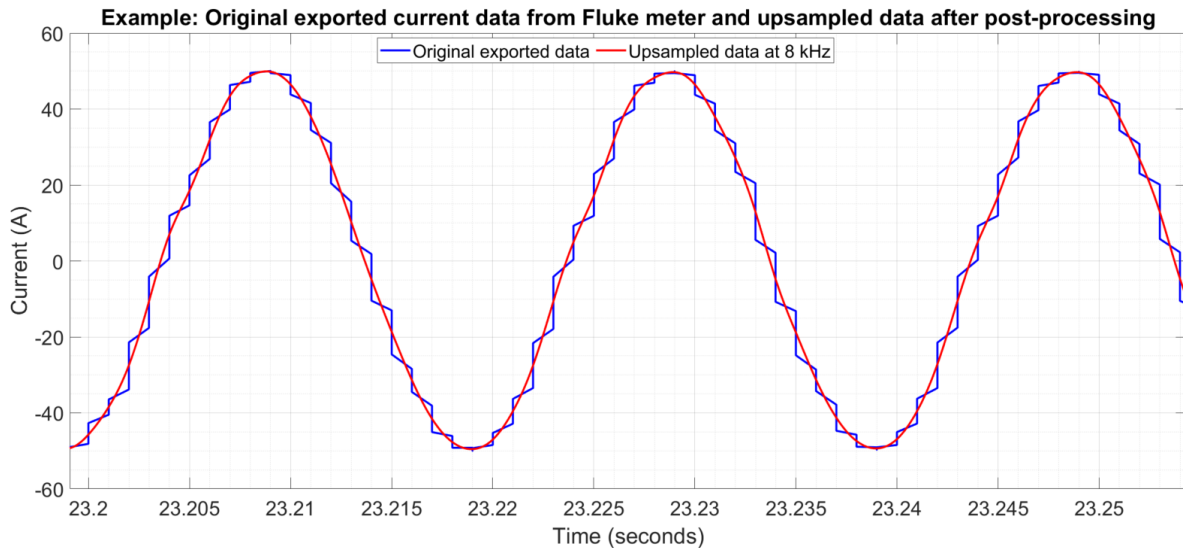


Figure 44: Comparison of measured Fluke data and up sampled data after post-processing using developed MATLAB script.

A.2. Post-processing measurement data from Beckhoff Data Acquisition System

Plotting the timeseries Beckhoff data revealed that the Beckhoff Data Acquisition System captures outliers in the measurement data. These outliers distort the waveshape of measured currents and voltages. Therefore, to remove the outliers from each measured quantity, a MATLAB script was developed which does the following:

1. Identifies outliers from the measured line voltages and currents using a moving window with median filtering.
2. Perform linear interpolation to replace the outliers in the data. This preserves the waveshape of the signal.

Figure 45 shows an example of the outliers measured and removed in the measured data. The outliers were removed and replaced after post-processing the measured data using the developed MATLAB script. The interpolation technique avoids distortion in the waveforms and maintains the trend in the waveshape. This was an important step before analysing the results from the Beckhoff Data Acquisition System.

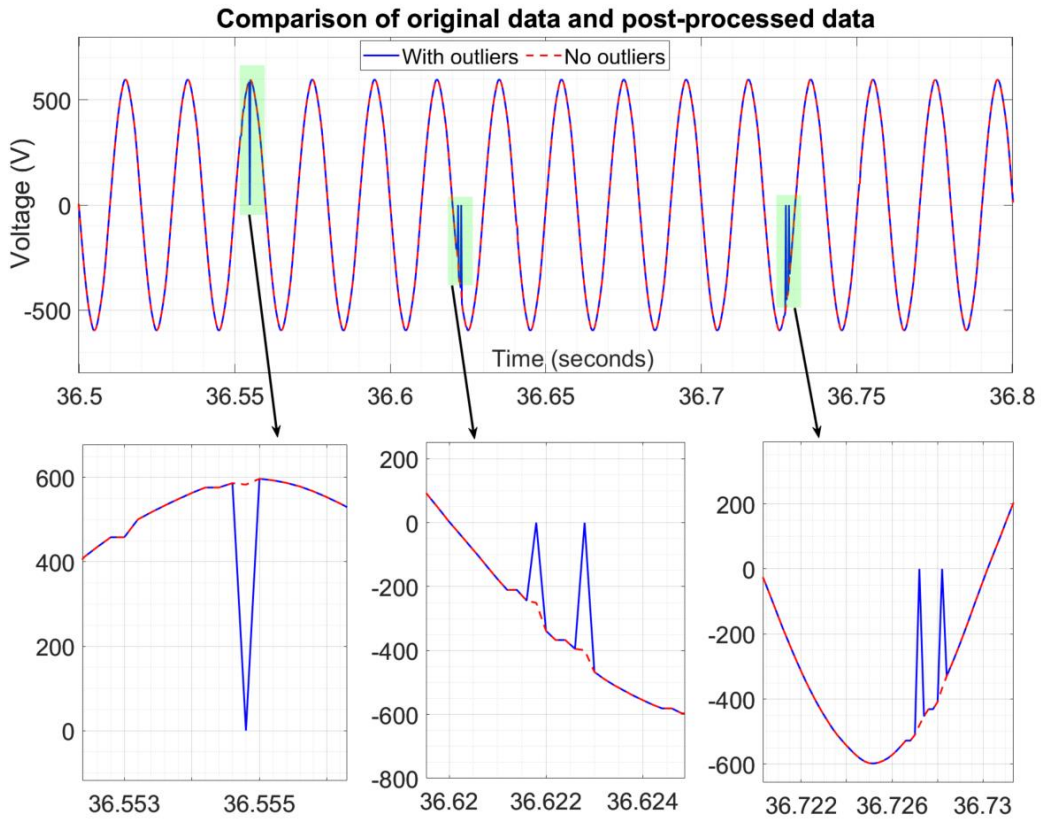


Figure 45: Comparison of original data with outliers and post-processed data after removing outliers

The post-processing steps were applied to each measurement set from the Fluke and Beckhoff Data Acquisition System, The MATLAB post-processing scripts for all meters were combined. The resulting MATLAB script is shown in Appendix C. MATLAB script for post-processing and time synchronisation.

Appendix B. Time-synchronisation of Fluke and Beckhoff Data Acquisition Systems

B.1. Test C1 - Synchronise Fluke D1 and Beckhoff D1

The end of compensation was first identified by the voltage spike in Fluke D1 and Beckhoff D1 measurements. The voltage V_{AB} measured by the two meters was plotted as shown in Figure 46. Time $t = 0$ s for each meter was identified by the GPS timestamp at which the meter starts measuring. Note that the Beckhoff Data Acquisition System measures “before compensation”, “during compensation” and “after compensation” time intervals whereas the Fluke meter measures “with compensation” and “after compensation” time intervals.

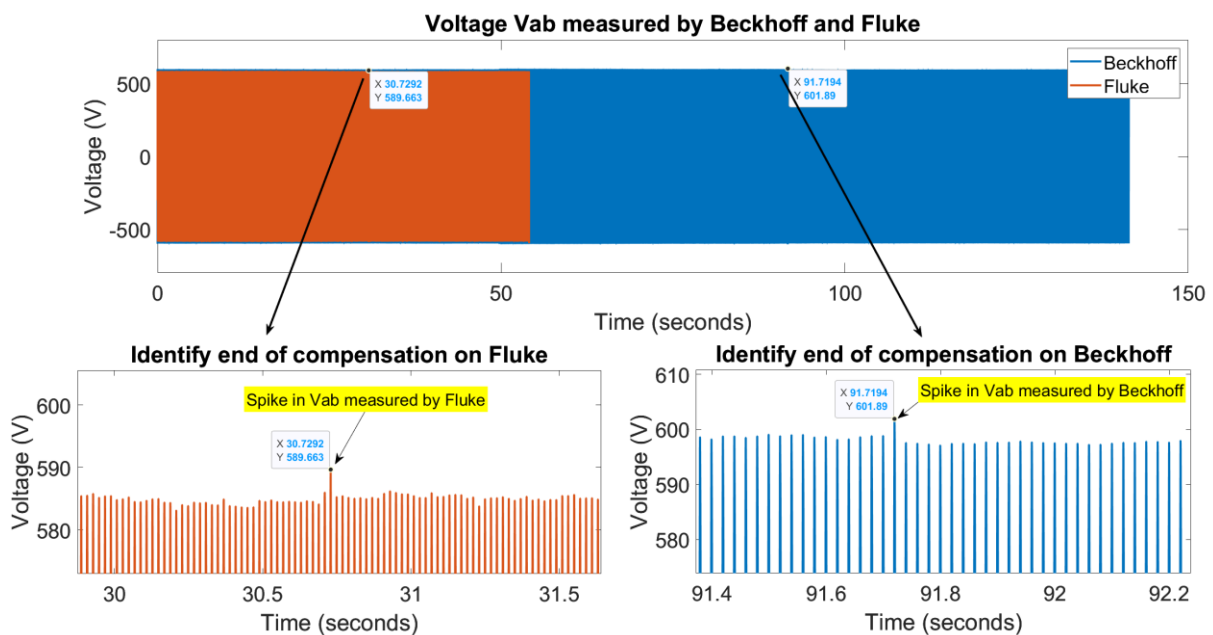


Figure 46: Test C1 - Unsynchronised voltage V_{AB} measured by Fluke and Beckhoff (bottom left waveform is in Fluke D1 seconds $s(F_{D1})$ and bottom right waveform is in Beckhoff D1 seconds $s(B_{D1})$)

End of compensation time from V-spike in Fluke = 30.7292 s(F_{D1})

End of compensation time from V-spike in Beckhoff = 91.7194 s(B_{D1})

Approximate time shift to apply to Beckhoff D1 measurements = 30.7292 s - 91.7194 s = - 60.9902 s

A more accurate end of compensation time can be identified from the Fluke measurements. The time at which Fluke D1 currents (compensating currents) become zero is chosen as the end of compensation time.

Currents become zero at 11:00:38:692 GPS(F_{D1}) = 30.745 s(F_{D1}) [See Figure 47]

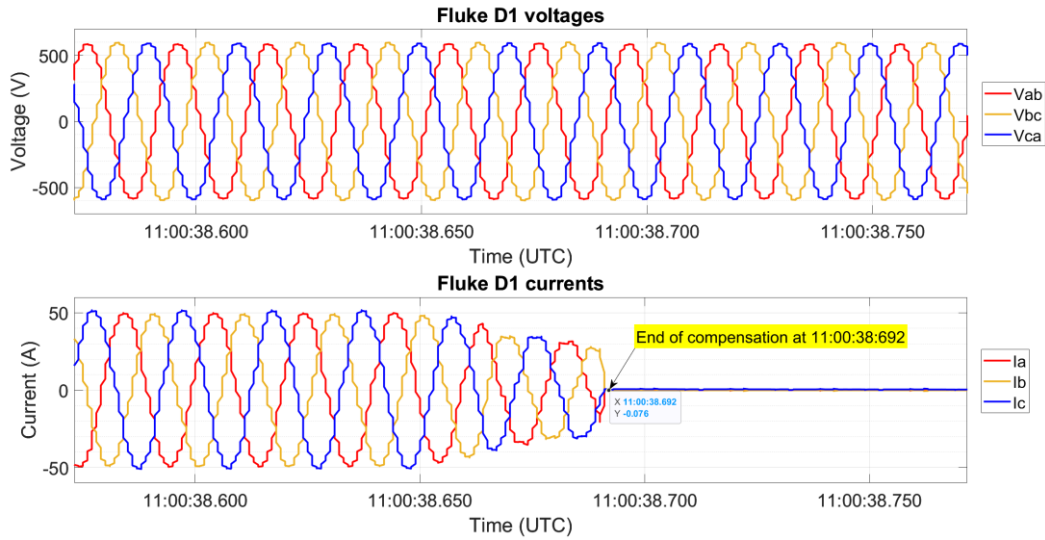


Figure 47: Test C1 - Fluke voltages and currents plotted to find end of compensation time.

The approximate time shift between voltage spikes identified from Figure 46 was subtracted from Beckhoff measurements. Then, the first red-positive-going zero crossing before the end of compensation time was chosen to find a perfect sync between Fluke and Beckhoff. This process is illustrated in Figure 48.

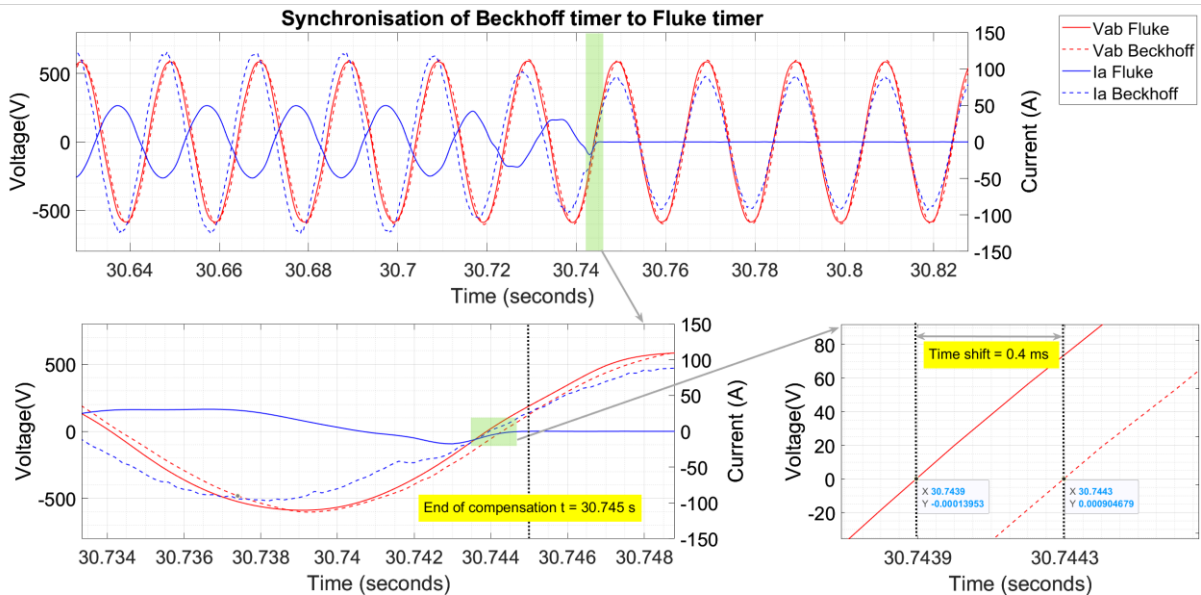


Figure 48: Test C1 - Synchronisation of Beckhoff and Fluke (top plot shows voltages and currents after being synchronised using the voltage spikes as reference, bottom left plot shows a zoomed-in image of the green-highlighted area from the top plot; it identifies the first zero-crossing the Fluke and Beckhoff voltages, before the end of compensation time, the bottom right plot shows a zoomed-in image of the bottom left; it identifies the time shift between the zero crossings. Time in s(F_{D1})

To match zero crossing of V_{ab} measured by Beckhoff D1 to Fluke D1, a time offset of 0.4 ms was required. Therefore, the exact time shift that must be applied to the Beckhoff measurements is:

Exact time shift to apply to Beckhoff D1 measurements = - 60.9902 s - 0.0004 s = - 60.9906 s

The synchronisation instant is $T_{sync} = 30.7439$ s(F_{D1}) and 91.7345 s(B_{D1}).

Figure 49 shows the synchronised Fluke D1 and Beckhoff D1 voltages and currents after

applying the time shift of - 60.9906 s to the Beckhoff measurements. A very good correlation was observed between the common Fluke and Beckhoff voltages. The low correlation at the peak is a result of post-processing of the Fluke measurements which tends to distort the waveform.

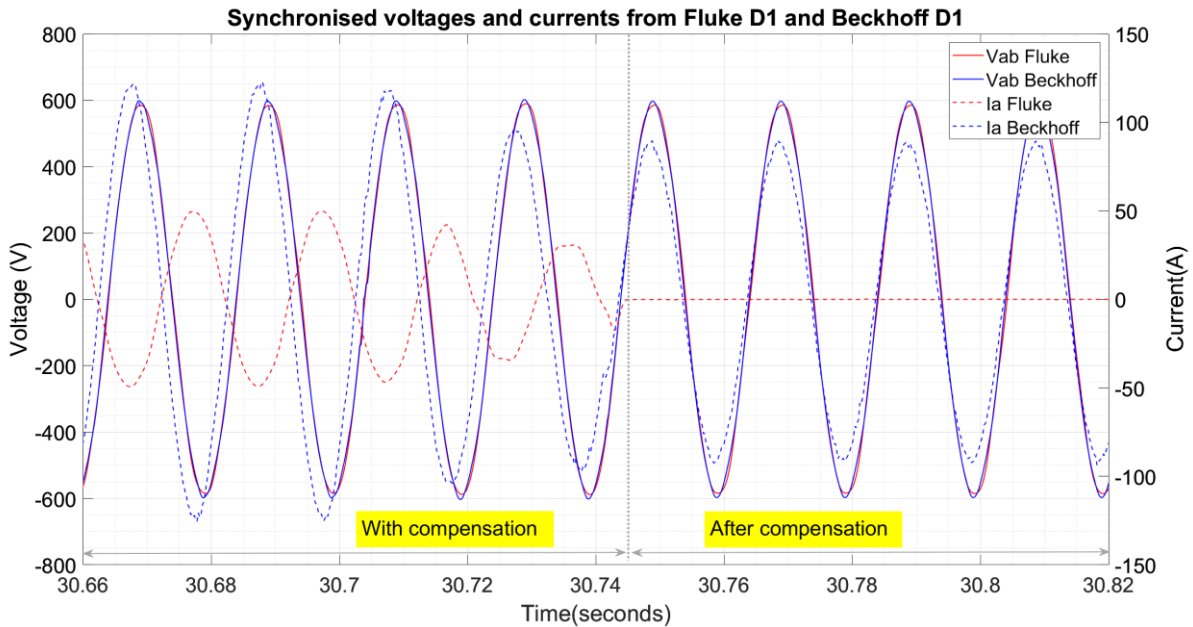


Figure 49: Test C1 - Synchronised Beckhoff and Fluke voltages and currents after zero-crossing matching. Time in $s(F_{D1})$.

B.2. Test C1 - Synchronise Fluke F2, F1 and Beckhoff Data Acquisition Systems

Simulations using MATLAB Simulink have shown that the cable capacitance has negligible effect on the network response. Since the network was modelled as a radial feeder with loads at bus 3 only, currents at all buses must be in phase. In other words, the current measured by Fluke meters F1 and F2, and Beckhoff Data Acquisition System D1 in each wire must be in phase. Therefore, Beckhoff D1 currents can be used to synchronise Fluke meters F1 and F2 first around the end of compensation in $s(B_{D1})$, then during time intervals before and after the end of compensation.

Figure 50 shows the currents measured by Beckhoff D1, Fluke F1 and Fluke F2 before any synchronisation was applied. Therefore, the currents are shown with a time-axis specific to each meter. The synchronisation instant identified from the Beckhoff D1 voltage's zero crossing was 91.7345 in $s(B_{D1})$. From Figure 50, it was observed that the zero-crossing of the Beckhoff D1 currents was at 91.73415834 s which is not equal to the voltage's zero-crossing. Hence Fluke F1 and F2 currents were synchronised to Beckhoff D1 currents by identifying the corresponding zero-crossing on the Fluke currents as shown by the plots in the right hand side of Figure 50.

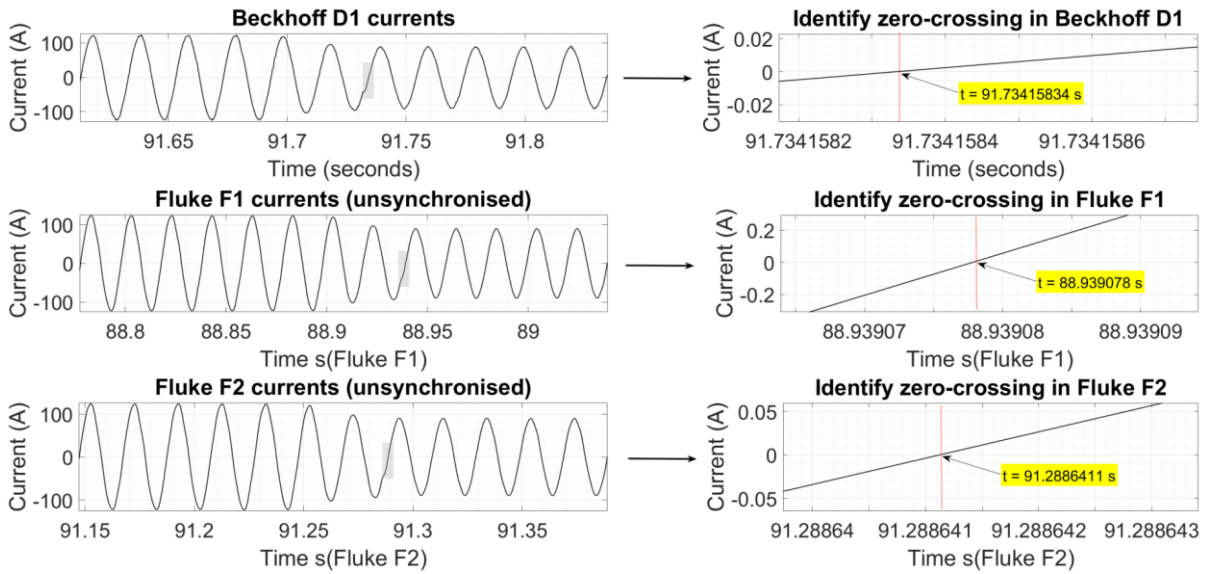


Figure 50: Test C1 - Identify the zero crossing in currents measured by Beckhoff D1, Fluke F1 and Fluke F2 around the end of compensation.

Zero-crossing in Beckhoff D1 current occurs at time $t = 91.73415834$ s(B_{D1})

Zero-crossing in Fluke F1 current occurs at time $t = 88.939078$ s(F_{F1})

Zero-crossing in Fluke F2 current occurs at time $t = 91.2886411$ s(F_{F2})

Time shift to apply to Fluke F1 to align to the Beckhoff D1 = 91.73415834 s – 88.939078 s = 2.79508034 s

Time shift to apply to Fluke F2 to align to the Beckhoff D1 = 91.73415834 s – 91.2886411 s = 0.44551724 s

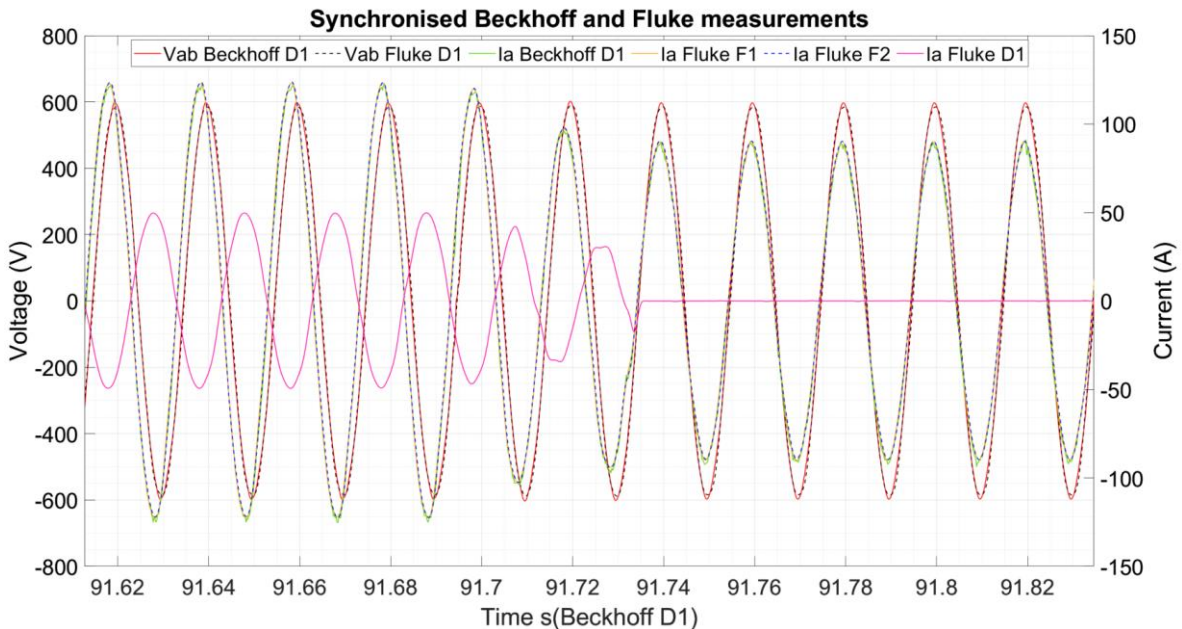


Figure 51: Test C1 - Synchronised Beckhoff D1, Fluke F1 and Fluke F2 measurements around the end of compensation

To analyse the results before, during and after compensation, it was necessary to identify four 3-cycle time intervals as described in Table B2.1.

Table 75: Description of chosen time intervals for analysing the results (Applies both to tests C1 and C2)

Time interval	Description
Before compensation t1	Time 5 cycles before start of compensation
During compensation t2	Time long enough after comp start for the system to have settled
During compensation t3	Time 10 cycles before end of compensation
After compensation t4	Time 5 cycles after end of compensation

To identify time interval t1, the time at which the converter was switched on was approximated (due to absence of data from Fluke D1 which measures the compensating currents) from the Beckhoff D1 phase A current waveform. The approximated time was 49.7785 s. The first positive going Fluke F1 current zero crossing was identified as $t = 49.773962$ s.

Then, 5 cycles before the peak at 49.7785 s was chosen by identifying the 5th positive going zero crossing before $t = 49.773962$ s. The time interval t1 was then chosen as 3-cycles from the identified 5th zero-crossing.

Figure 52 shows the process of identifying time interval t1. Figure 53 show the process of identifying time interval t2.

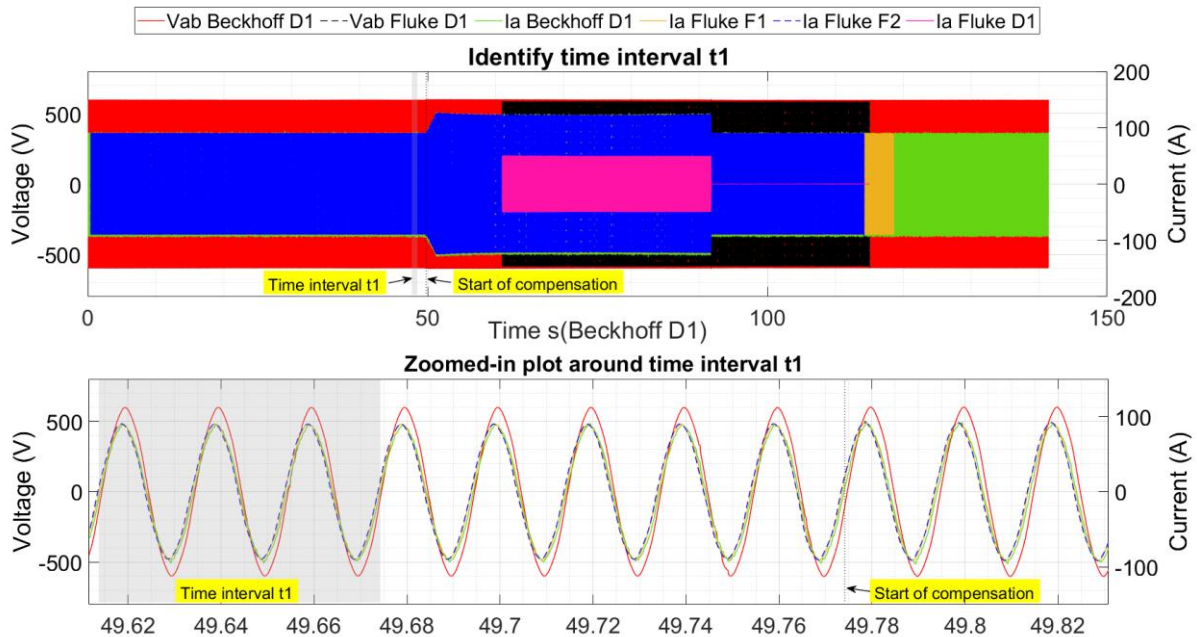


Figure 52: Test C1 - Identifying time interval t1 before compensation

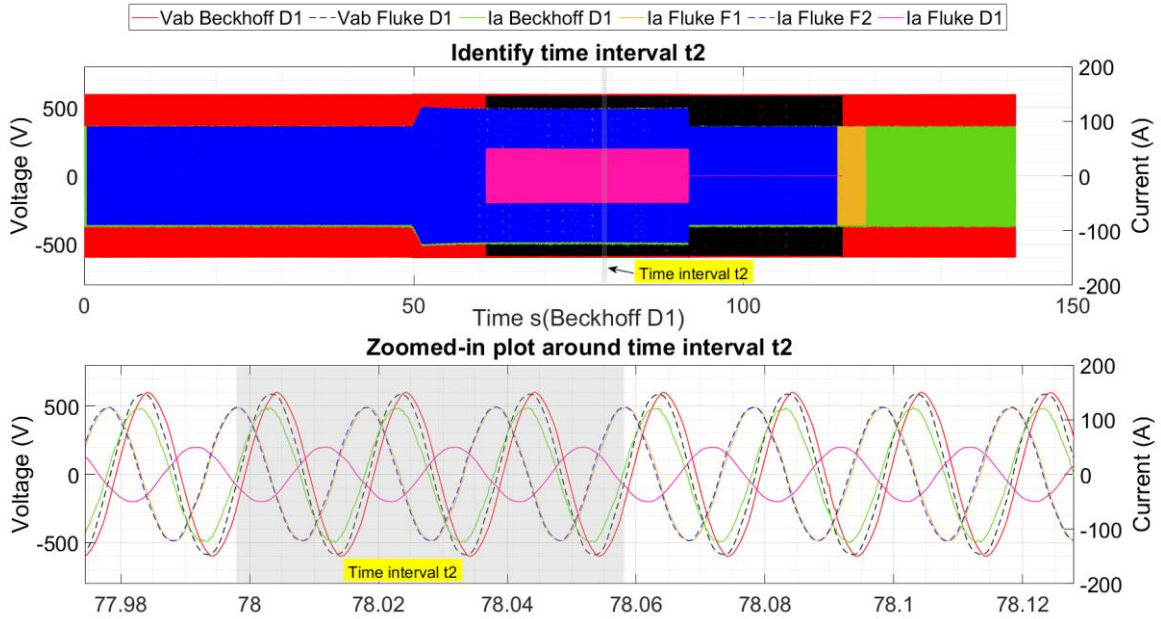


Figure 53: Test C1 - Identifying time interval t_2 during compensation

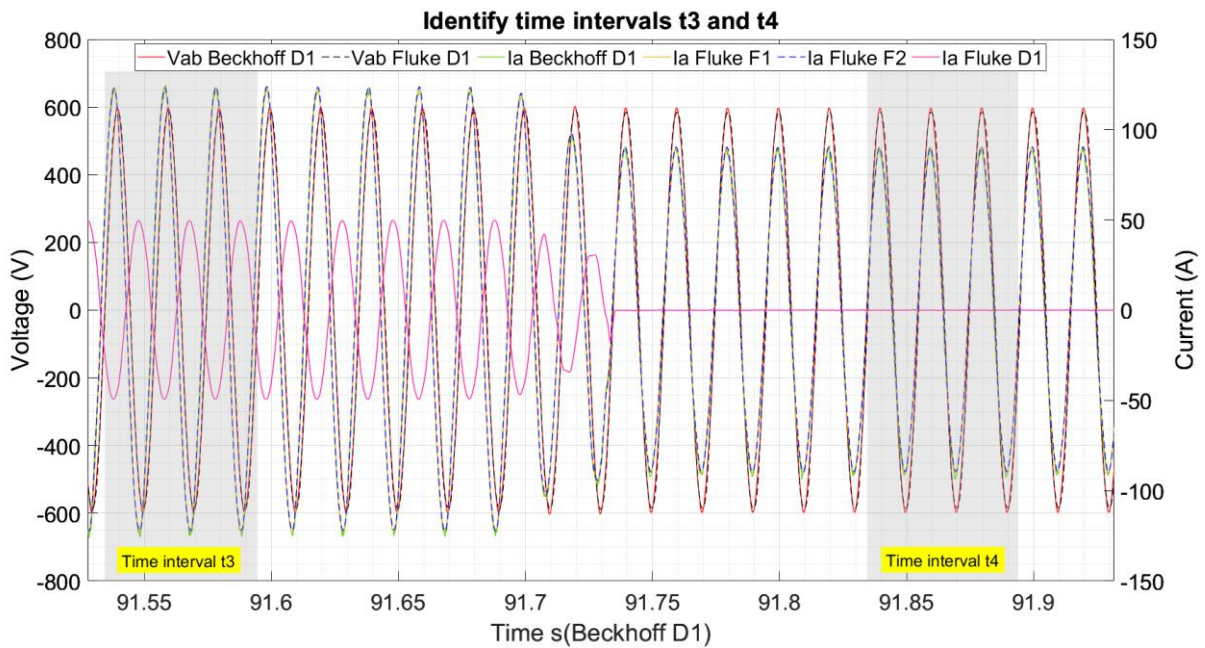


Figure 54: Test C1 - Identifying time intervals t_3 and t_4 - before and after compensation respectively

Even though the meters were synchronised around the end of compensation instant (Figure 51), an apparent timer drift was observed in all meters. The Beckhoff timer drifted the most over time as compared to the Fluke meters. Therefore, the Beckhoff current measurements were used as reference to find an additional time shift that must be applied to the Fluke meters for perfect synchronisation in each time interval. Table 76 summaries the resulting time shifts applied to each meter during each time interval used for analysis.

Table 76: Test C1 – Resulting time shifts or correction factors to apply to Fluke measurements such that they align to the Beckhoff measurements during different time intervals used for analysis

Time interval	Fluke F2	Fluke F1	Fluke D1
Synchronisation instant (Fig B2.2)	0.44551724	2.79508034	60.9906
t1	0.44616154	2.79543057	NA
t2	0.45034126	2.79972207	60.99149193
t3	0.44549579	2.79521722	60.9905491
t4	0.44548381	2.79521496	60.99043921

The identified time intervals in each meter's own time in seconds are given in Table 77. The frequency of the system during the 3-cycle time intervals was calculated from the currents by taking the inverse of the difference in time of the first positive going zero crossing to the third positive going zero-crossing.

Table 77: Test C1 - Time intervals for analysis in $s(B_{D1})$, $s(F_{F1})$, $s(F_{F2})$ and frequency used for FFT.

Time intervals	Identified times $s(B_{D1})$	Identified times $s(F_{F1})$	Identified times $s(F_{F2})$	Frequency from 3-cycle average (Hz)
t1	[49.773961, 49.834028]	[49.773611, 49.833678]	[49.773317, 49.8333842]	49.944195
t2	[77.997883, 78.057918]	[77.993241, 78.053276]	[79.993059, 80.053094]	49.970975
t3	[91.534408, 91.594452]	[88.739191, 88.799234]	[91.088912, 91.1489562]	49.963360
t4	[91.834569, 91.894618]	[89.039354, 89.099403]	[91.389085, 91.449134]	49.959200

B.3. Test C2 - Synchronise Fluke D1 and Beckhoff Data Acquisition Systems

During post-processing of test C1 measurement data, the end of compensation was first identified by identifying the voltage spike in Fluke D1 and Beckhoff D1 measurements. During post-processing of test C2 measurement data, the voltage spike was only observed from Beckhoff D1 voltage measurements. Fluke D1 did not capture the voltage spike, possibly because the variable sampling frequency missed the data points representing the spike.

Figure 55 shows the voltage V_{AB} measured by Fluke D1 and Beckhoff D1 before applying any synchronisation or time shift to align the measurements.

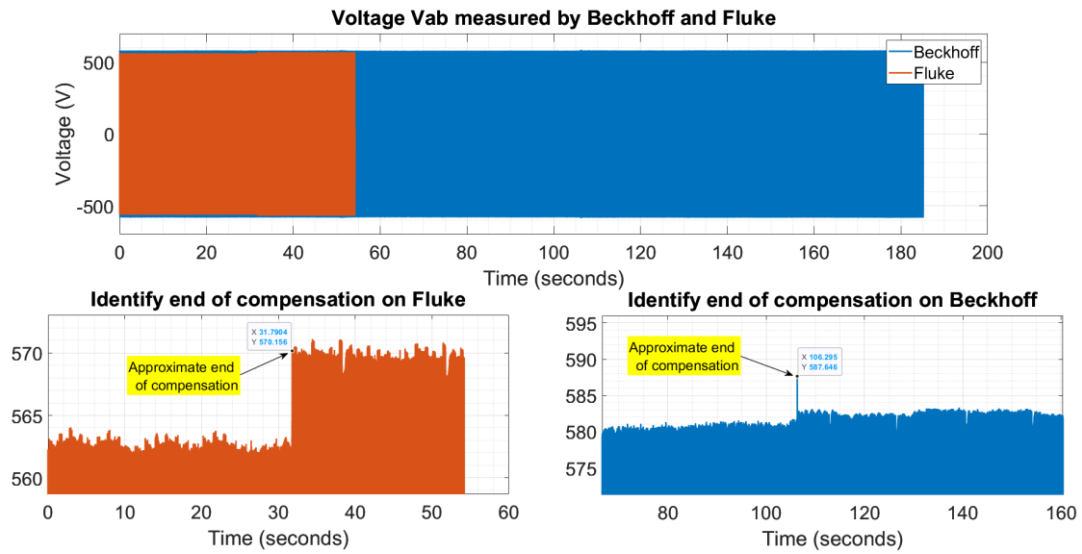


Figure 55: Test C2 - Unsynchronised voltage V_{AB} measured by Fluke and Beckhoff (bottom left waveform is in Fluke D1 seconds $s(F_{D1})$ and bottom right waveform is in Beckhoff D1 seconds $s(B_{D1})$)

End of compensation time from V-spike in Fluke = 31.7904 s(F_{D1})

End of compensation time from V-spike in Beckhoff = 106.295 s(B_{D1})

Approximate time shift to apply to Beckhoff D1 measurements = 31.7904 s – 106.295 s = - 74.5046 s

A more accurate end of compensation time can be identified from the Fluke current measurements. The time at which Fluke D1 currents (compensating currents) become zero is chosen as the end of compensation time.

Currents become zero at $t= 31.779$ s(F_{D1}) as shown in Figure 56.

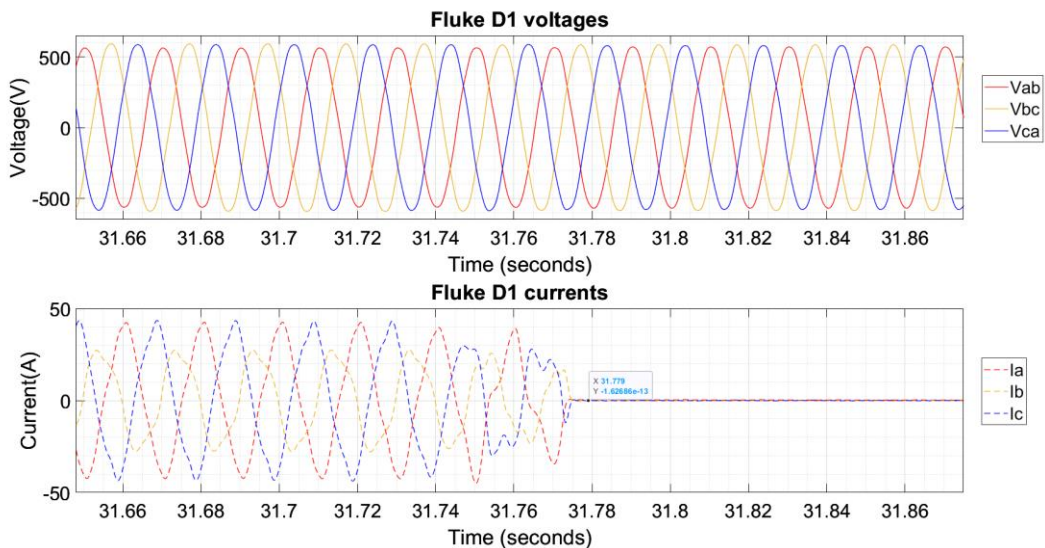


Figure 56: Test C2 - Unsynchronised voltage V_{AB} measured by Fluke and Beckhoff (bottom left waveform is in Fluke D1 seconds $s(F_{D1})$ and bottom right waveform is in Beckhoff D1 seconds $s(B_{D1})$)

The approximate time shift between voltage spikes identified from Figure 55 was subtracted

from Beckhoff measurements. Then, the first red-positive-going zero crossing before the end of compensation time identified from Fluke D1 currents, was chosen to find a perfect sync between Fluke and Beckhoff. This process is shown in Figure 57.

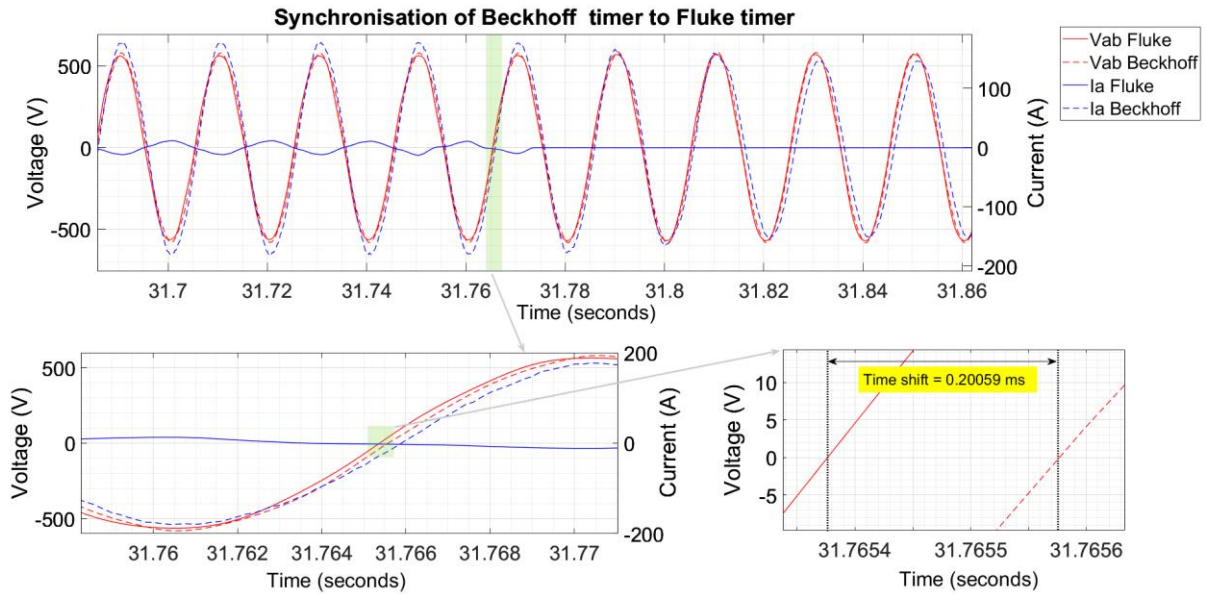


Figure 57: Test C2 - Synchronisation of Beckhoff and Fluke (top plot shows voltages and currents after being synchronised using the voltage spikes as reference, bottom left plot shows a zoomed-in image of the green-highlighted area from the top plot; it identifies the first zero-crossing the Fluke and Beckhoff voltages, before the end of compensation time identified from Fluke D1 currents, the bottom right plot shows a zoomed-in image of the bottom left plot; it identifies the time shift between the zero crossings. Time in s(F_{D1})

To match zero crossing of V_{ab} measured by Beckhoff D1 to Fluke D1, a time offset of 0.20059 ms was required. Therefore, the exact time shift that must be applied to the Beckhoff measurements is:

$$\text{Exact time shift to apply to Beckhoff D1 measurements} = - 74.5046 \text{ s} - 0.20059 \text{ ms} = - 74.50480059 \text{ s}$$

The synchronisation instant is $T_{\text{sync}} = 31.7653762 \text{ s}(F_{D1})$ and $106.2701768 \text{ s}(B_{D1})$.

Figure 58 shows the synchronised Fluke D1 and Beckhoff D1 voltages and currents after applying the time shift of - 60.9906 s to the Beckhoff measurements. A very good correlation was observed between the common Fluke and Beckhoff voltages. The low correlation at the peak is a result of post-processing of the Fluke measurements which tends to distort the waveform.

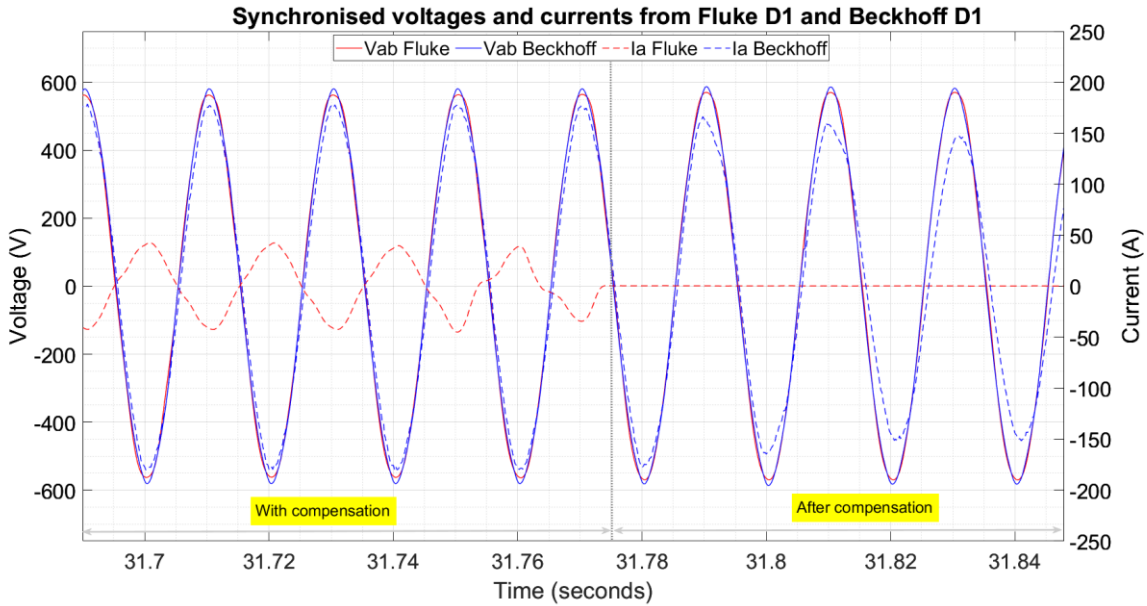


Figure 58: Test C2 - Synchronised Beckhoff and Fluke voltages and currents after zero-crossing matching. Time in $s(F_{D1})$.

B.4. Test C2 - Synchronise Fluke F2, F1 and Beckhoff Data Acquisition Systems

Like test C1, Beckhoff D1 currents were used to synchronise Fluke meters F1 and F2 first around the end of compensation in $s(B_{D1})$, then during time intervals before and after the end of compensation.

Figure 59 shows the currents measured by Beckhoff D1, Fluke F1 and Fluke F2 before any synchronisation was applied. Therefore, the currents are shown with a time-axis specific to each meter. The synchronisation instant identified from the Beckhoff D1 voltage's zero crossing was 106.2701768 in $s(B_{D1})$. From Figure 59, it was observed that the zero-crossing of the Beckhoff D1 currents was at 91.73415834 s which is not equal to the voltage's zero-crossing. Hence Fluke F1 and F2 currents were synchronised to Beckhoff D1 currents by identifying the corresponding zero-crossing on the Fluke currents as shown by the plots in the right hand side of Figure 59.

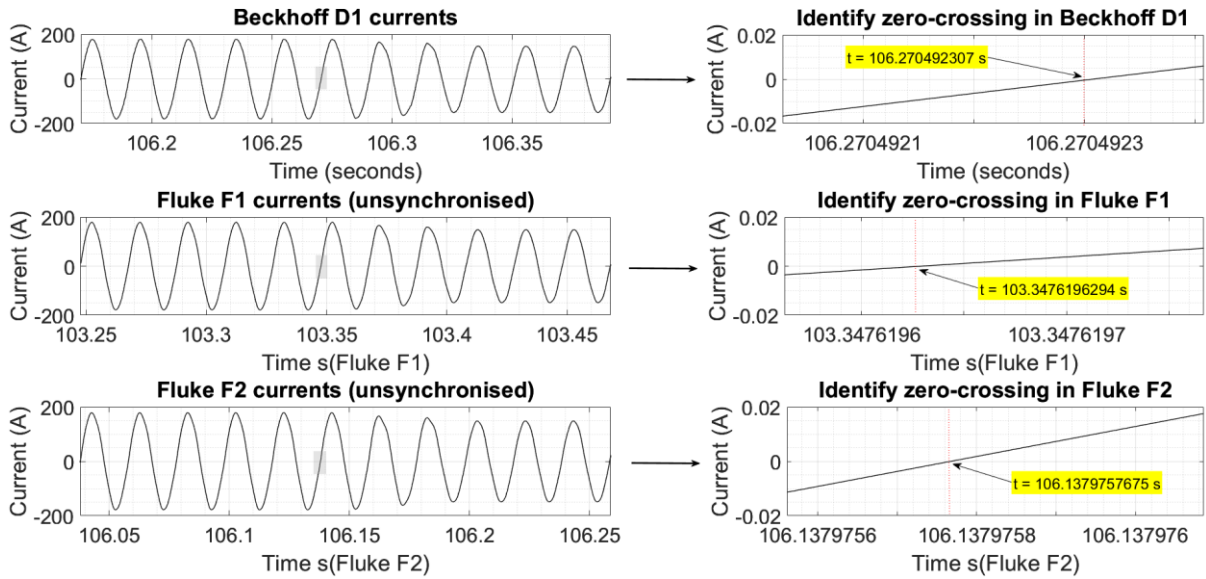


Figure 59: Test C2 - Identify the zero crossing in currents measured by Beckhoff D1, Fluke F1 and Fluke F2 around the end of compensation.

Zero-crossing in Beckhoff D1 current occurs at time $t = 106.270492307$ s(B_{D1})

Zero-crossing in Fluke F1 current occurs at time $t = 103.3476196294$ s(F_{F1})

Zero-crossing in Fluke F2 current occurs at time $t = 106.1379757675$ s(F_{F2})

Time shift to apply to Fluke F1 to align to the Beckhoff D1 = 106.270492307 s – 103.3476196294 s = 2.9228727 s

Time shift to apply to Fluke F2 to align to the Beckhoff D1 = 106.270492307 s – 106.1379757675 s = 0.1325166 s

Figure 60 shows the synchronised Beckhoff D1 and Fluke D1 measurements around the end of compensation.

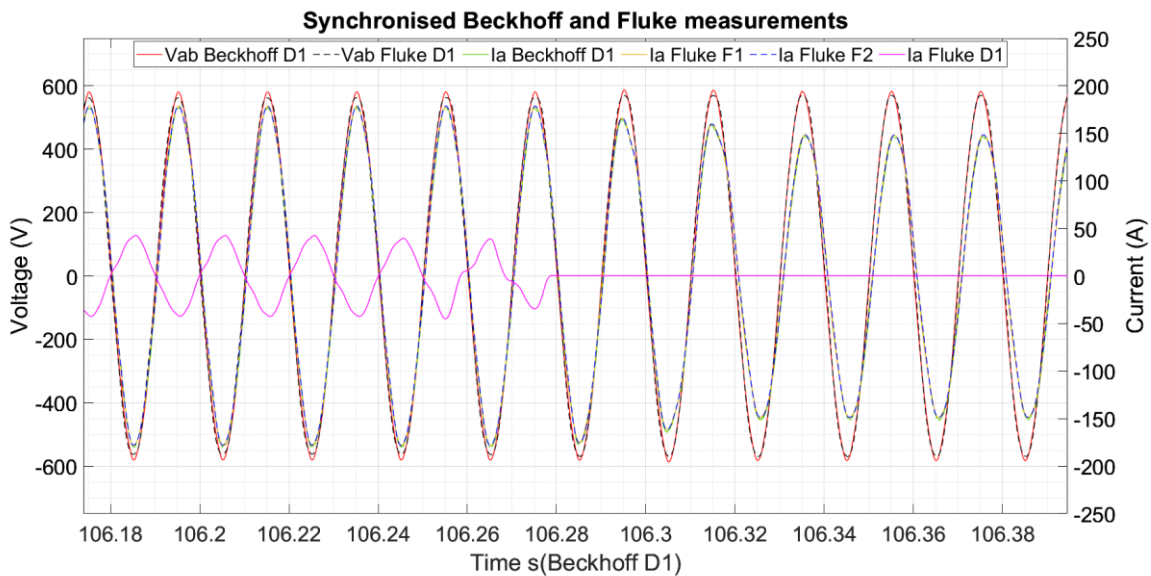


Figure 60: Test C2 - Synchronised Beckhoff D1 and Fluke D1 measurements around the end of compensation instant

To analyse the results before, during and after compensation, it was necessary to identify four

3-cycle time intervals. The same conditions as test C1 (Refer to Table B2.1) were used to identify the time intervals for analysis.

To identify time interval t_1 , the time at which the converter was switched on was approximated (due to absence of data from Fluke D1 which measures the compensating currents) from the Beckhoff D1 phase A current waveform. The approximated time was 50.8191 s. The first positive going Fluke F1 current zero crossing was identified as $t = 50.8148$ s.

Then, 5 cycles before the peak at 50.6598 s was chosen by identifying the 5th positive going zero crossing before $t = 50.6548$ s. The time interval t_1 was then chosen as 3-cycles from the identified 5th zero-crossing as shown in Figure 61. Figure 62 and Figure 63 illustrate time intervals t_2 , t_3 and t_4 respectively.

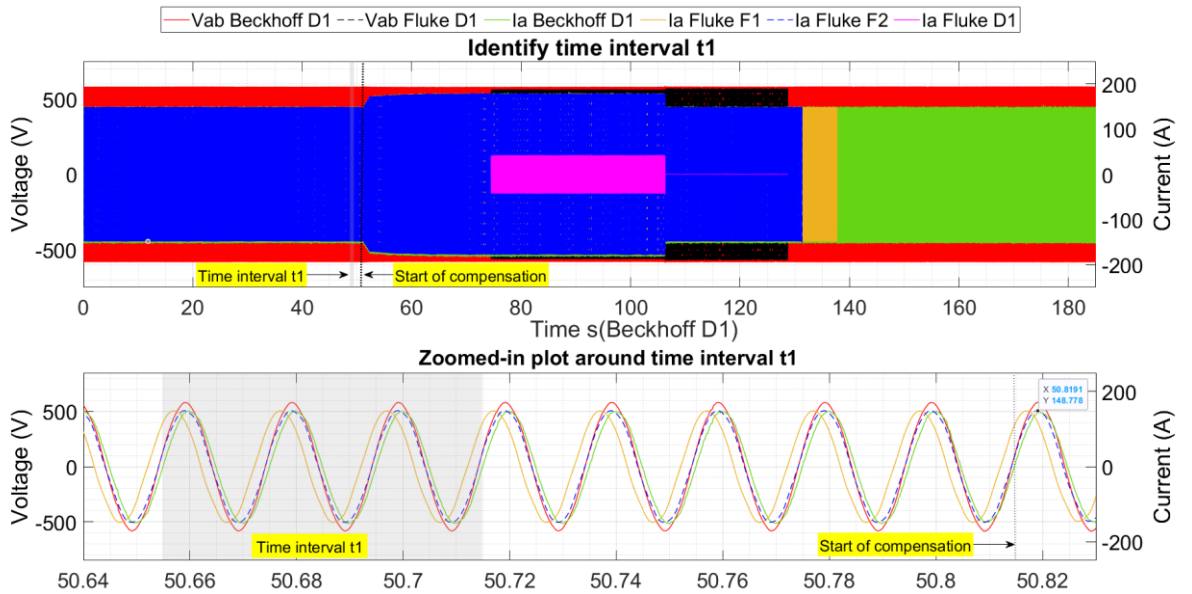


Figure 61: Test C2 - Identifying time interval t_1 before compensation

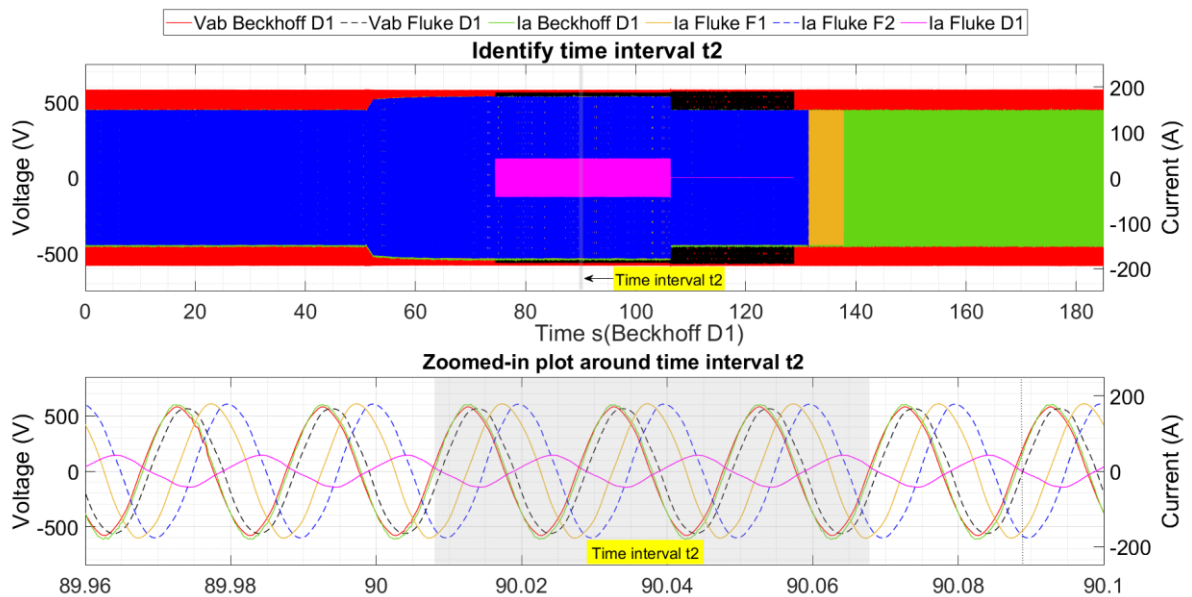


Figure 62: Test C2 - Identifying time interval t_2 during compensation.

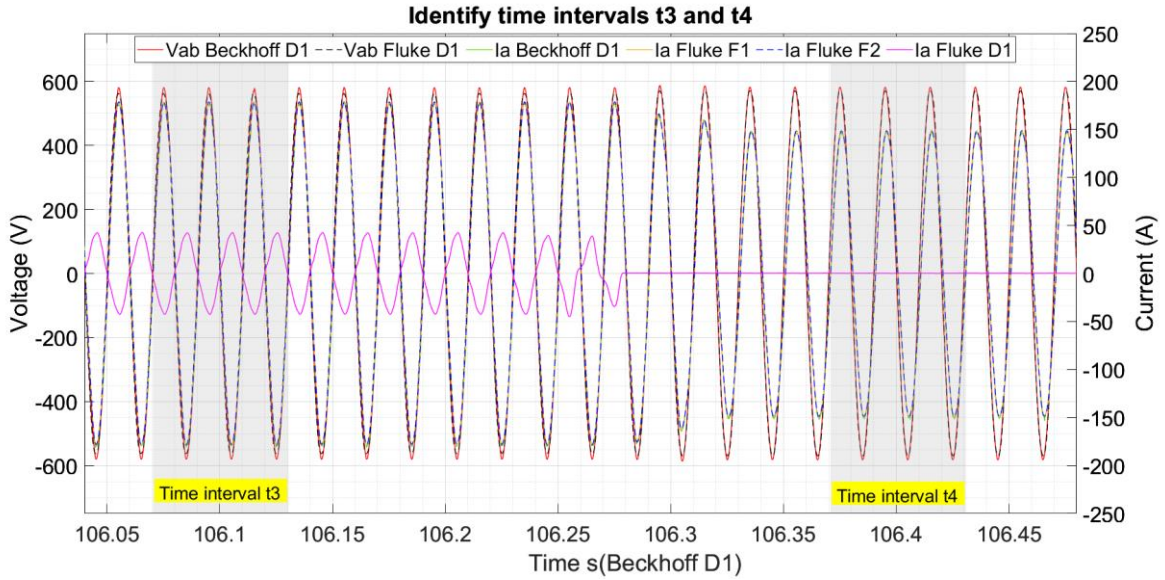


Figure 63: Test C2 - Identifying time intervals t3 and t4, before and after compensation respectively.

As in test C1, an apparent timer drift was observed in all meters. Table 78 summaries the resulting time shifts applied to each meter during each time interval used for analysis.

Table 78: Test C2 - Resulting time shifts or correction factors to apply to Fluke measurements such that they align to the Beckhoff measurements during different time intervals used for analysis

Time interval	Fluke F1	Fluke F2	Fluke D1
Synchronisation instant (Fig B2.11)	2.9228727	0.1325166	74.50480059
t1	2.92573247	0.13331544	NA
t2	2.91826651	0.12565802	74.50353531
t3	2.9229034	0.1324997	74.50481849
t4	2.9229957	0.1325527	74.50474129

The identified time intervals in each meter’s own time in seconds are given in Table 79. The frequency of the system during the 3-cycle time intervals was calculated from the Beckhoff D1 currents by taking the inverse of the difference in time of the first positive going zero crossing to the third positive going zero-crossing.

Table 79: Test C2 - Time intervals for analysis in $s(B_{D1})$, $s(F_{F1})$, $s(F_{F2})$ and frequency used for FFT.

Time intervals	Identified times $s(B_{D1})$	Identified times $s(F_{F1})$	Identified times $s(F_{F2})$	Frequency from 3-cycle average (Hz)
t1	[50.6549357142, 50.71493103448]	[47.72920324, 47.78919856]	[50.52162027, 50.58161559]	50.0039003
t2	[90.0079209302, 90.0679743589]	[87.08965442, 87.14970784]	[89.88226291, 89.94231633]	49.9555229
t3	[106.070550, 106.1302254587]	[103.1476466, 103.207322]	[105.9380503, 105.9977257]	50.2719714
t4	[106.3709375, 106.430897142]	[103.4479418, 103.5079014]	[106.2383848, 106.2983444]	50.0336894

B.1. Investigation of Beckhoff timer drift

The Fluke measurements are more trust-worthy since they are GPS-time stamped. The Beckhoff Data Acquisition System was not calibrated and therefore we suspected a timer drift problem in the meter. We therefore used an approach of identifying six 250-cycle periods before and after the reference zero crossing identified from the end of compensation, in both Fluke and Beckhoff voltages. For example, the Beckhoff average frequency measured is around 49.95 Hz. 250-cycles of 49.95 Hz gives a time period of 5.005 s. Six such 5.005 s periods were then marked and the exact (times) periods of the 250 cycles between zero crossings occur were measured according to the Beckhoff timer. The higher Fluke frequency and lower period of about 5.004 s gave similarly the exact times, but GPS time-stamped. The ratio between the time periods identified on the Beckhoff to the time periods identified on the Fluke gives an indication of the timer drift. The results are shown in Figure 64.

Table 80 indicates that the drift in Beckhoff was found to be slow and small enough to be corrected by matching with waveforms recorded by the GPS linked Fluke meter.

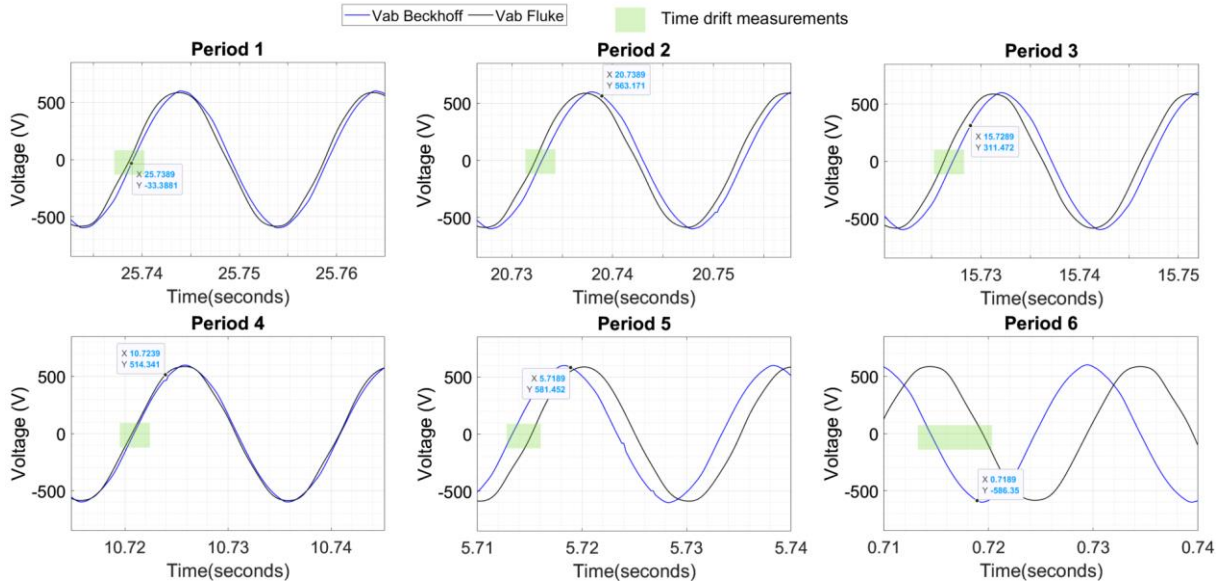


Figure 64: Fluke D1 and Beckhoff D1 voltages during different periods after synchronisation shows that there is a drift in the Beckhoff Data Acquisition System over time.

Table 80: Results from the analysis of the Beckhoff timer drift showing a small ratio of the cycle-periods measured by Beckhoff D1 and Fluke D1.

Period #	From/to s(B)	Actual found at s(B)	T(B) ms	From s(F)	Found at s(F)	T(F) ms	Ratio of T(B)/T(F)
0	91.7345 (act.)	--		30.7439	--	--	
Before zero-crossing							
-1	86.7295 (est)	86.7297	5.0048	25.7399 (est)	25.7387	5.0052	0.99992
-2	81.7247	81.7236	5.0061	20.7347	20.7323	5.0064	0.99994
-3	76.7186	76.7177	5.0059	15.7283	15.7262	5.0085	0.99948
-4	71.7127	71.7115	5.0062	10.7222	10.7207	5.0055	1.00014
-5	66.7065	66.7039	5.0076	5.71670	5.71519	5.0055	1.00042
-6	61.6989	61.6950	5.0089	0.71119	0.70935	5.0058	1.00062
After zero-crossing							
+1	96.7395	96.7389	5.0044	35.7479	35.7503	5.0064	0.99960
+2	101.744	101.746	5.0071	40.7543	40.7578	5.0075	0.99992
+3	106.751	106.752	5.0061	45.7618	45.7636	5.0058	1.00005
+4	111.757	111.757	5.0050	50.7676	50.7688	5.0052	0.99996
+5	116.762	116.769	5.0120	No data from Fluke after t = 54.0678 s			
+6	121.774	121.781	5.0120				

Appendix C. MATLAB script for post-processing and time synchronisation

The MATLAB scripts used for post-processing the measured data for an example test case is shown in this Appendix. Note that correction factors applicable for different time intervals identified to analyse the results were also specified in the script.

```

% Project: ERI Grid - AGI Demo
% Author: Pitambar Jankee
% Rev: 3

%Frequency for FFT Analysis
% F = 50.0039003 in time interval t1
% F = 49.9555229 in time interval t2
% F = 50.2719714 in time interval t3
% F = 50.0336894 in time interval t4
f = 50.2719714;

% -----%
%                               Read data from Fluke F2                               %
% -----%

% Load data from text file
dataF2 = readtable('TestC2_F2_Measurements', 'Delimiter', '\t', 'HeaderLines', 1);

% Clean up time strings and convert to numerical format
time_arrayF2 = dataF2(:, 2);
VabF2 = dataF2(:, 3);
VbcF2 = dataF2(:, 4);
VcaF2 = dataF2(:, 5);
IaF2 = dataF2(:, 6);
IbF2 = dataF2(:, 7);
IcF2 = dataF2(:, 8);
time_strF2 = string(time_arrayF2);

% Replace commas with dots
VabF2 = strrep(VabF2, ',', '.');
VbcF2 = strrep(VbcF2, ',', '.');
VcaF2 = strrep(VcaF2, ',', '.');
IaF2 = strrep(IaF2, ',', '.');
IbF2 = strrep(IbF2, ',', '.');
IcF2 = strrep(IcF2, ',', '.');

% Convert to array
VabF2 = str2double(VabF2);
VbcF2 = str2double(VbcF2);
VcaF2 = str2double(VcaF2);
IaF2 = str2double(IaF2);
IbF2 = str2double(IbF2);
IcF2 = str2double(IcF2);

% Convert time to seconds
time_strF2 = regexp(time_strF2, '(\d\d):(\d\d):(\d\d)\.(\d+)', '$1:$2:$3.$4');
time_secF2 = datenum(time_strF2, 'HH:MM:SS.FFF');

```

```

time_secF2 = (time_secF2 - time_secF2(1)) * 86400;

% Find unique time points
[unique_timeF2, iaF2, icF2] = unique(time_secF2);

% Compute average V, I for each unique time point
Vab_avgF2 = accumarray(icF2, VabF2, [], @mean);
Vbc_avgF2 = accumarray(icF2, VbcF2, [], @mean);
Vca_avgF2 = accumarray(icF2, VcaF2, [], @mean);
Ia_avgF2 = accumarray(icF2, IaF2, [], @mean);
Ib_avgF2 = accumarray(icF2, IbF2, [], @mean);
Ic_avgF2 = accumarray(icF2, IcF2, [], @mean);

% Upsample voltage data
fs_new = 5000; % New sampling rate in Hz
Vab_upsampledF2 = interp(Vab_avgF2, fs_new / (1/1e-3));
Vbc_upsampledF2 = interp(Vbc_avgF2, fs_new / (1/1e-3));
Vca_upsampledF2 = interp(Vca_avgF2, fs_new / (1/1e-3));
Ia_upsampledF2 = interp(Ia_avgF2, fs_new / (1/1e-3));
Ib_upsampledF2 = interp(Ib_avgF2, fs_new / (1/1e-3));
Ic_upsampledF2 = interp(Ic_avgF2, fs_new / (1/1e-3));

% Generate timeseries for F2 data
tF2=(0:length(Vab_upsampledF2)-1) / fs_new;
tF2=tF2';
VabF2_timeseries=timeseries(Vab_upsampledF2,tF2);
VbcF2_timeseries=timeseries(Vbc_upsampledF2,tF2);
VcaF2_timeseries=timeseries(Vca_upsampledF2,tF2);
IaF2_timeseries=timeseries(Ia_upsampledF2,tF2);
IbF2_timeseries=timeseries(Ib_upsampledF2,tF2);
IcF2_timeseries=timeseries(Ic_upsampledF2,tF2);

% F2 correction factors
% During time interval t1, correction factor = 0.13331544
% During time interval t2, correction factor = 0.12565802
% During time interval t3, correction factor = 0.1324997
% During synchronisation instant, correction factor = 0.1325166
% During time interval t4, correction factor = 0.1325527
F_F2_Correction_Factor = 0.1325527;
Vab_F2_Fluke=timeseries(Vab_upsampledF2,tF2+F_F2_Correction_Factor);
Vbc_F2_Fluke=timeseries(Vbc_upsampledF2,tF2+F_F2_Correction_Factor);
Vca_F2_Fluke=timeseries(Vca_upsampledF2,tF2+F_F2_Correction_Factor);
Ia_F2_Fluke=timeseries(Ia_upsampledF2,tF2+F_F2_Correction_Factor);
Ib_F2_Fluke=timeseries(Ib_upsampledF2,tF2+F_F2_Correction_Factor);
Ic_F2_Fluke=timeseries(Ic_upsampledF2,tF2+F_F2_Correction_Factor);

% -----%
%                               Read data from Fluke F1                               %
% -----%

% Load data from text file
dataF1 = readtable('TestC2_F1_Measurements', 'Delimiter', '\t', 'HeaderLines', 1);

% Clean up time strings and convert to numerical format
time_arrayF1 = dataF1{:, 2};
VabF1 = dataF1{:, 3};
VbcF1 = dataF1{:, 4};
VcaF1 = dataF1{:, 5};
IaF1 = dataF1{:, 6};

```

```

IbF1 = dataF1{:, 7};
IcF1 = dataF1{:, 8};
time_strF1 = string(time_arrayF1);

% Replace commas with dots
VabF1 = strrep(VabF1, ',', '.');
VbcF1 = strrep(VbcF1, ',', '.');
VcaF1 = strrep(VcaF1, ',', '.');
IaF1 = strrep(IaF1, ',', '.');
IbF1 = strrep(IbF1, ',', '.');
IcF1 = strrep(IcF1, ',', '.');

% Convert to array
VabF1 = str2double(VabF1);
VbcF1 = str2double(VbcF1);
VcaF1 = str2double(VcaF1);
IaF1 = str2double(IaF1);
IbF1 = str2double(IbF1);
IcF1 = str2double(IcF1);

% Convert time to seconds
time_strF1 = regexp(time_strF1, '(\d\d):(\d\d):(\d\d)\.(\d+)', '$1:$2:$3.$4');
time_secF1 = datenum(time_strF1, 'HH:MM:SS.FFF');
time_secF1 = (time_secF1 - time_secF1(1)) * 86400;

% Find unique time points
[unique_timeF1, iaF1, icF1] = unique(time_secF1);

% Compute average V, I for each unique time point
Vab_avgF1 = accumarray(icF1, VabF1, [], @mean);
Vbc_avgF1 = accumarray(icF1, VbcF1, [], @mean);
Vca_avgF1 = accumarray(icF1, VcaF1, [], @mean);
Ia_avgF1 = accumarray(icF1, IaF1, [], @mean);
Ib_avgF1 = accumarray(icF1, IbF1, [], @mean);
Ic_avgF1 = accumarray(icF1, IcF1, [], @mean);

% Upsample voltage data
fs_new = 5000; % New sampling rate in Hz
Vab_upsampledF1 = interp(Vab_avgF1, fs_new / (1/1e-3));
Vbc_upsampledF1 = interp(Vbc_avgF1, fs_new / (1/1e-3));
Vca_upsampledF1 = interp(Vca_avgF1, fs_new / (1/1e-3));
Ia_upsampledF1 = interp(Ia_avgF1, fs_new / (1/1e-3));
Ib_upsampledF1 = interp(Ib_avgF1, fs_new / (1/1e-3));
Ic_upsampledF1 = interp(Ic_avgF1, fs_new / (1/1e-3));

% Generate timeseries for F1 data
tF1=(0:length(Vab_upsampledF1)-1) / fs_new;
tF1=tF1';
VbaF1_timeseries=timeseries(Vab_upsampledF1,tF1);
VbcF1_timeseries=timeseries(Vbc_upsampledF1,tF1);
VcaF1_timeseries=timeseries(Vca_upsampledF1,tF1);
IaF1_timeseries=timeseries(Ia_upsampledF1,tF1);
IbF1_timeseries=timeseries(Ib_upsampledF1,tF1);
IcF1_timeseries=timeseries(Ic_upsampledF1,tF1);

% F1 correction factors
% During time interval t1, correction factor = 2.92573247
% During time interval t2, correction factor = 2.91826651
% During time interval t3, correction factor = 2.9229034

```

```

% During synchronisation instant, correction factor = 2.9228727
% During time interval t4, correction factor = 2.9229957
F_F1_Correction_Factor = 2.9229034;
Vab_F1_Fluke=timeseries(Vab_upsampledF1,tF1+F_F1_Correction_Factor);
Vbc_F1_Fluke=timeseries(Vbc_upsampledF1,tF1+F_F1_Correction_Factor);
Vca_F1_Fluke=timeseries(Vca_upsampledF1,tF1+F_F1_Correction_Factor);
Ia_F1_Fluke=timeseries(Ia_upsampledF1,tF1+F_F1_Correction_Factor);
Ib_F1_Fluke=timeseries(Ib_upsampledF1,tF1+F_F1_Correction_Factor);
Ic_F1_Fluke=timeseries(Ic_upsampledF1,tF1+F_F1_Correction_Factor);

% -----
%                               Read data from Fluke D1                               %
% -----

% Load data from text file
dataD1 = readtable('TestC2_D1_Measurements', 'Delimiter', '\t', 'HeaderLines', 1);

% Clean up time strings and convert to numerical format
time_arrayD1 = dataD1{:, 2};
VabD1 = dataD1{:, 3};
VbcD1 = dataD1{:, 4};
VcaD1 = dataD1{:, 5};
IaD1 = dataD1{:, 6};
IbD1 = dataD1{:, 7};
IcD1 = dataD1{:, 8};
time_strD1 = string(time_arrayD1);

% Replace commas with dots
VabD1 = strrep(VabD1, ',', '.');
VbcD1 = strrep(VbcD1, ',', '.');
VcaD1 = strrep(VcaD1, ',', '.');
IaD1 = strrep(IaD1, ',', '.');
IbD1 = strrep(IbD1, ',', '.');
IcD1 = strrep(IcD1, ',', '.');

% Convert to array
VabD1 = str2double(VabD1);
VbcD1 = str2double(VbcD1);
VcaD1 = str2double(VcaD1);
IaD1 = str2double(IaD1);
IbD1 = str2double(IbD1);
IcD1 = str2double(IcD1);

% Convert time to seconds
time_strD1 = regexp(time_strD1, '(\d\d):(\d\d):(\d\d)\.(\d+)', '$1:$2:$3.$4');
time_secD1 = datenum(time_strD1, 'HH:MM:SS.FFF');
time_secD1 = (time_secD1 - time_secD1(1)) * 86400;

% Find unique time points
[unique_timeD1, iaD1, icD1] = unique(time_secD1);

% Compute average V, I for each unique time point
Vab_avgD1 = accumarray(icD1, VabD1, [], @mean);
Vbc_avgD1 = accumarray(icD1, VbcD1, [], @mean);
Vca_avgD1 = accumarray(icD1, VcaD1, [], @mean);
Ia_avgD1 = accumarray(icD1, IaD1, [], @mean);
Ib_avgD1 = accumarray(icD1, IbD1, [], @mean);
Ic_avgD1 = accumarray(icD1, IcD1, [], @mean);

```

```

% Upsample voltage data
fs_new = 5000; % New sampling rate in Hz
Vab_upsampledD1 = interp(Vab_avgD1, fs_new / (1/1e-3));
Vbc_upsampledD1 = interp(Vbc_avgD1, fs_new / (1/1e-3));
Vca_upsampledD1 = interp(Vca_avgD1, fs_new / (1/1e-3));
Ia_upsampledD1 = interp(Ia_avgD1, fs_new / (1/1e-3));
Ib_upsampledD1 = interp(Ib_avgD1, fs_new / (1/1e-3));
Ic_upsampledD1 = interp(Ic_avgD1, fs_new / (1/1e-3));

% Generate timeseries for D1 data
tD1=(0:length(Vab_upsampledD1)-1) / fs_new;
tD1=tD1';
VabD1_timeseries=timeseries(Vab_upsampledD1,tD1);
VbcD1_timeseries=timeseries(Vbc_upsampledD1,tD1);
VcaD1_timeseries=timeseries(Vca_upsampledD1,tD1);
IaD1_timeseries=timeseries(Ia_upsampledD1,tD1);
IbD1_timeseries=timeseries(Ib_upsampledD1,tD1);
IcD1_timeseries=timeseries(Ic_upsampledD1,tD1);

% D1 correction factors
% During time interval t2, correction factor = 74.50353531
% During time interval t3, correction factor = 74.50481849
% During synchronisation instant, correction factor = 74.50480059
% During time interval t4, correction factor = 74.50474129
F_D1_Correction_Factor = 74.50481849;
Vab_D1_Fluke=timeseries(Vab_upsampledD1,tD1+F_D1_Correction_Factor);
Vbc_D1_Fluke=timeseries(Vbc_upsampledD1,tD1+F_D1_Correction_Factor);
Vca_D1_Fluke=timeseries(Vca_upsampledD1,tD1+F_D1_Correction_Factor);
Ia_D1_Fluke=timeseries(Ia_upsampledD1,tD1+F_D1_Correction_Factor);
Ib_D1_Fluke=timeseries(Ib_upsampledD1,tD1+F_D1_Correction_Factor);
Ic_D1_Fluke=timeseries(Ic_upsampledD1,tD1+F_D1_Correction_Factor);

% -----%
%                               Read data from Beckhoff D1                               %
% -----%

% Read the data from the CSV file
dataD1_Beckhoff = csvread('Meas29.csv', 26, 1); % Assuming there are 26 header
rows and starting from column 2

% Extract the specific columns and assign them to variables
IaD1_Beckhoff = dataD1_Beckhoff(:, 1); % Column 2
IbD1_Beckhoff = dataD1_Beckhoff(:, 3); % Column 4
IcD1_Beckhoff = dataD1_Beckhoff(:, 5); % Column 6
VabD1_Beckhoff = dataD1_Beckhoff(:, 7); % Column 8
VbcD1_Beckhoff = dataD1_Beckhoff(:, 9); % Column 10
VcaD1_Beckhoff = dataD1_Beckhoff(:, 11); % Column 12

% Calculate the time vector based on the sampling frequency
samplingFrequency = 5000; % 5 kHz
t = (0:size(dataD1_Beckhoff, 1)-1) / samplingFrequency;

% Set the threshold value for outlier identification
threshold=100;

% Set the window size for median filtering (adjust as needed)
windowSize = 4;

%-----%
AGIPDEM

```

```

% -----REMOVE OUTLIERS FROM VAB -----%
%-----%

% Apply median filtering
Vab_median = medfilt1(VabD1_Beckhoff, windowSize);

% Identify outliers
Vab_outliers = abs(VabD1_Beckhoff - Vab_median) > threshold;

% Perform linear interpolation for outlier replacement
Vab_clean = VabD1_Beckhoff;
Vab_clean(Vab_outliers) = interp1(t(~Vab_outliers), Vab_median(~Vab_outliers),
t(Vab_outliers));

%-----%
% -----REMOVE OUTLIERS FROM VBC -----%
%-----%

% Apply median filtering
Vbc_median = medfilt1(VbcD1_Beckhoff, windowSize);

% Identify outliers
Vbc_outliers = abs(VbcD1_Beckhoff - Vbc_median) > threshold;

% Perform linear interpolation for outlier replacement
Vbc_clean = VbcD1_Beckhoff;
Vbc_clean(Vbc_outliers) = interp1(t(~Vbc_outliers), Vbc_median(~Vbc_outliers),
t(Vbc_outliers));

%-----%
% -----REMOVE OUTLIERS FROM VCA -----%
%-----%

% Apply median filtering
Vca_median = medfilt1(VcaD1_Beckhoff, windowSize);

% Identify outliers
Vca_outliers = abs(VcaD1_Beckhoff - Vca_median) > threshold;

% Perform linear interpolation for outlier replacement
Vca_clean = VcaD1_Beckhoff;
Vca_clean(Vca_outliers) = interp1(t(~Vca_outliers), Vca_median(~Vca_outliers),
t(Vca_outliers));

%-----%
% -----REMOVE OUTLIERS FROM IA -----%
%-----%

% Apply median filtering
Ia_median = medfilt1(IaD1_Beckhoff, windowSize);

% Identify outliers
Ia_outliers = abs(IaD1_Beckhoff - Ia_median) > threshold;

% Perform linear interpolation for outlier replacement
Ia_clean = IaD1_Beckhoff;
Ia_clean(Ia_outliers) = interp1(t(~Ia_outliers), Ia_median(~Ia_outliers),
t(Ia_outliers));

```

```

%-----%
% -----REMOVE OUTLIERS FROM IB -----%
%-----%

% Apply median filtering
Ib_median = medfilt1(IbD1_Beckhoff, windowSize);

% Identify outliers
Ib_outliers = abs(IbD1_Beckhoff - Ib_median) > threshold;

% Perform linear interpolation for outlier replacement
Ib_clean = IbD1_Beckhoff;
Ib_clean(Ib_outliers) = interp1(t(~Ib_outliers), Ib_median(~Ib_outliers),
t(Ib_outliers));

%-----%
% -----REMOVE OUTLIERS FROM IC -----%
%-----%

% Apply median filtering
Ic_median = medfilt1(IcD1_Beckhoff, windowSize);

% Identify outliers
Ic_outliers = abs(IcD1_Beckhoff - Ic_median) > threshold;

% Perform linear interpolation for outlier replacement
Ic_clean = IcD1_Beckhoff;
Ic_clean(Ic_outliers) = interp1(t(~Ic_outliers), Ic_median(~Ic_outliers),
t(Ic_outliers));

% Correction factor to align Fluke D1 to Beckhoff D1
% Correction factor = 0 for all time intervals

B_D1_Correction_Factor = 0;

% Generate timeseries when sync meters to voltage
Ia_D1_Beckhoff=timeseries(Ia_clean,t+B_D1_Correction_Factor);
Ib_D1_Beckhoff=timeseries(Ib_clean,t+B_D1_Correction_Factor);
Ic_D1_Beckhoff=timeseries(Ic_clean,t+B_D1_Correction_Factor);

Vab_D1_Beckhoff=timeseries(Vab_clean,t+B_D1_Correction_Factor);
Vbc_D1_Beckhoff=timeseries(Vbc_clean,t+B_D1_Correction_Factor);
Vca_D1_Beckhoff=timeseries(Vca_clean,t+B_D1_Correction_Factor);

```


Disclaimer

This document contains material, which is copyrighted by the authors and may not be reproduced or copied without permission.

The commercial use of any information in this document may require a licence from the proprietor of that information.

Neither the Lab Access User Group as a whole, nor any single person warrant that the information contained in this document is capable of use, nor that the use of such information is free from risk. Neither the Lab Access User Group as a whole, nor any single person accepts any liability for loss or damage suffered by any person using the information.

This document does not represent the opinion of the European Community, and the European Community is not responsible for any use that might be made of its content.

Copyright Notice

© 2021 by the authors, the Lab Access User Group.

